MOSTEK®

Z80 MICROCOMPUTER SYSTEMS

Operations Manual

FLP-80E FLEXIBLE DISK DRIVE CONTROLLER BOARD

OPERATIONS MANUAL

FOR

FLP–80E
FLEXIBLE DISK DRIVE CONTROLLER BOARD
(MK78112)

TABLE OF CONTENTS

TABLE OF CONTENTS CONTD.

TABLE OF CONTENTS CONTD.

LIST OF FIGURES

LIST OF TABLES

SECTION 1

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. The FLP-80E board (shown in Figure 1-1) is an add-on flexible disk drive controller for MOSTEK's SOFTWARE DEVELOPMENT SYSTEM. In addition to functioning as a add-on card to the software development system, the FLP-80E may be utilized directly in OEM applications to control/format up to four flexible disk drives of either single or dual sided types.

1-3. This manual references the drives used as Shugart SA800 single density - single sided and SA850 single density - dual sided. This is done strictly for tutorial purposes and does not imply that other manufacturers drive are not compatible.

1-4. The following hardware features are summarized below.

1. Soft Sector Format Compatible with IBM 3740 data entry system format.
2. Capable of controlling up to four flexible disk drives.
3. Double Sided Drive Capability.
4. Disk Initialization (Formating).
5. Full Sector (128 bytes) FIFO buffering for data, allowing real time operation.
6. Double buffering for control and status.
7. Automatic Track Seek with track verification.

1-5. The FLP-80E provides the necessary electronics to accomplish track selection, head loading, data transfer, error detection, flexible drive interface, status reporting and format generation/recognition.

1-6. FUNCTIONAL DESCRIPTION.

1-7. The FLP-80E board uses a MOS/LSI controller chip mated with a 128x8 bit FIFO to accomplish control and interfacing with up to four flexible disk drives in a real-time environment. The board is primarily designed for use with the MOSTEK (SDB) Software Development System in the MOSTEK AID STATION (AID-80F) using 2 SHUGART SA800 or 2 SHUGART SA850 type flexible disk drives. The board could however be used

in OEM applications with up to four flexible disk drives of SHUGART SA800/SA850 type or equivalent.

1-8. The 128x8 FIFO allows up to a full sector of buffering on both read and write operations to /from the disk. This configuration allows reading, writing, and disk formating (Initialization) of disk media without using interrupts or wait states. The controller board may be configured by means of a jumper option to generate a system interrupt for use with OEM applications where interrupts from this board might be desired.

1-9. Figure 1-2 is a block diagram of the FLP-80E board. The input buffer prevents excessive loading of the system bus. The pseudo switch before and after the FIFO allows a choice of paths to the controller chip which are:

1. FIFO buffered path; thru the FIFO for buffering.

2. Direct path; bypassing the FIFO.

The buffered path is used on both Read and Write operations to buffer up to a sector in length of data. The direct path is used for communicating commands where an immediate response is necessary. The direct path is also used for formatting when special restraints are added to the interrupt system and software to allow dedicated CPU control. The flexible disk formatter/controller chip performs the control/transfer functions of data, status, and control word transfers. Refer directly to paragraph 4-36 for definitions of these functions.

1-10. By means of PORT $E2_H$ and $E3_H$ (defined in paragraph 4-5), the CPU can control the direction and use of the FIFO. Bit 7 of PORT $E3_H$ controls the direction of data flow within the FIFO (i.e. "0" indicates Rd from FIFO to CPU). Bit 6 of PORT $E3_H$ directs data into the FIFO for buffering or around the FIFO for direct communication with the controller chip. FIFO buffering is used on read or write operations, while direct connection is necessary for commands and formatting. Bit 5 of port $E3_H$ is used to reset the FIFO to clear it of any unwanted data. Bit 4 of port $E3_H$ selects side 2 of dual sided configurations. Bits 0-3 of port $E3_H$ select drives 1 thru 4. Bit "0" of PORT $E2_H$ indicates which side of a double sided disk is being accessed. Bit 1 of PORT $E2_H$ indicates ("Interrupt") an end of operation or error condition exists. This prompts

Figure 1-1. FLP-80E Board.

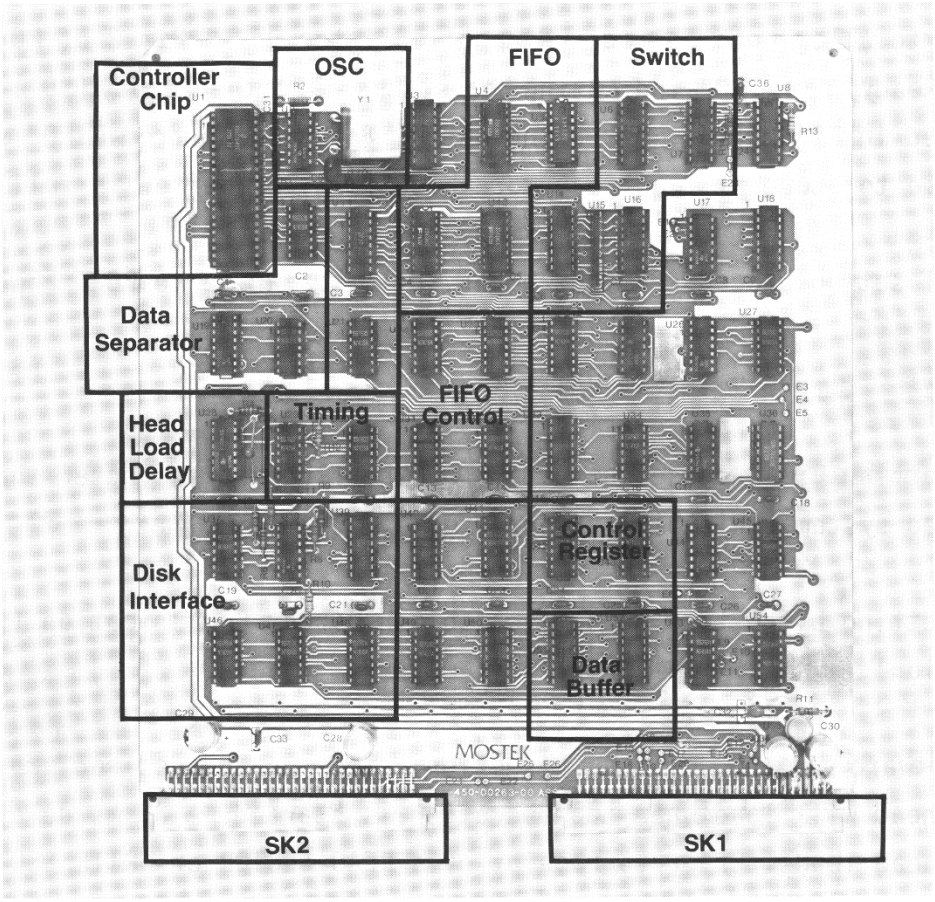
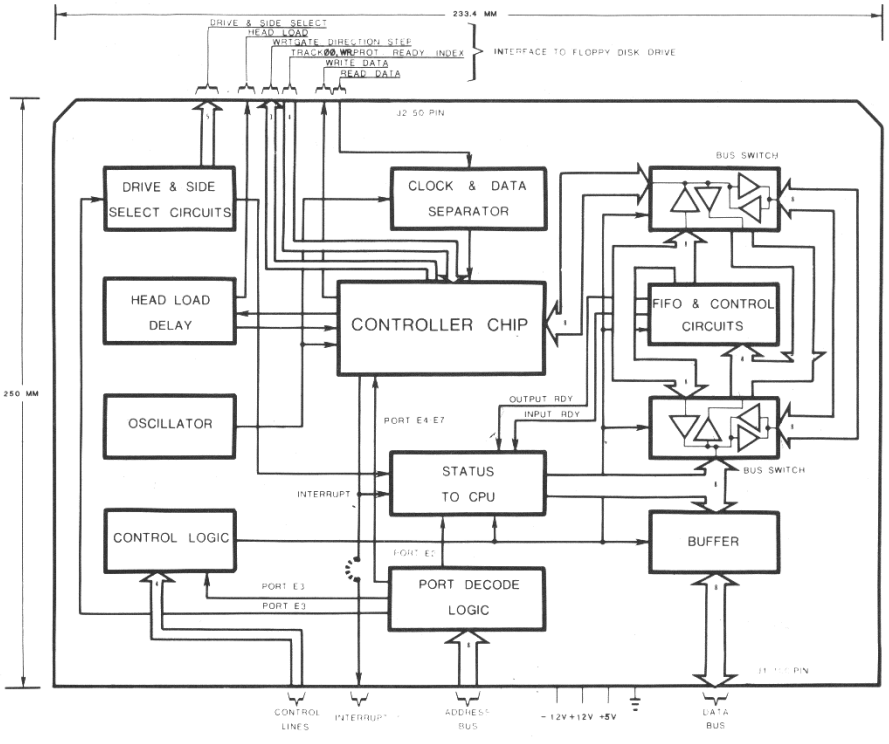


Figure 1-2. FLP-80E Block Diagram.



the CPU to read the status register of controller chip to determine the nature of interrupt. The interrupt signal is also available as a jumper option to interrupt the CTC on the SDB to allow both polled and unpolled interrupts. Bit 2 of PORT $E2_H$ indicates "Output Ready from FIFO" indicating the status is either empty ("0") or 1 to 128 bytes are stored in FIFO ("1"). Bit 3 indicates "Input Ready from FIFO" showing that the FIFO is able to store at least one more byte ("1") or buffer is full ("0").

A typical set up procedure might be as follows: Write to PORT $E3_H$,

Setting Bit Ø to select Drive 1

Resetting Bit 4 to select side 1 of the floppy disk (note: that on single sided systems this bit has no effect).

Resetting bit 6 to a zero to establish Direct Communication (vs FIFO action).

1-11. The software may now set the direction, step to the desired track and begin operation. The head will load when the operation is started. A 35 ms delay is experienced as the head loads. Prior to receipt of a READ SECTOR or WRITE SECTOR command, the SDB must load the sector register with the desired sector number. Upon receipt of a READ SECTOR or WRITE SECTOR command, the busy status bit of controller chip is set. If the E Flag = 1 (this is the normal case) the Head Load signal (HLD) is made active. This signal causes the head on the selected drive to load. After the 35 ms delay, the READ SECTOR or WRITE SECTOR will begin operation. The head will remain loaded until the controller receives a command that specifically disengages the head. If no commands are received after two revolutions of the disk, the head will automatically disengage.

1-12. ELECTRICAL DESCRIPTION.

1-13. INTERFACE. The FLP-80E is fully TTL compatible on inputs and outputs. Schmitt-trigger inputs provide good noise margins. Jumper options provide flexibility for use with other systems and port options.

1-14. Figure 1-3, System Diagram, and Figure 1-4 ,System Interconnection Diagram, show

Figure 1-3. System Diagram.

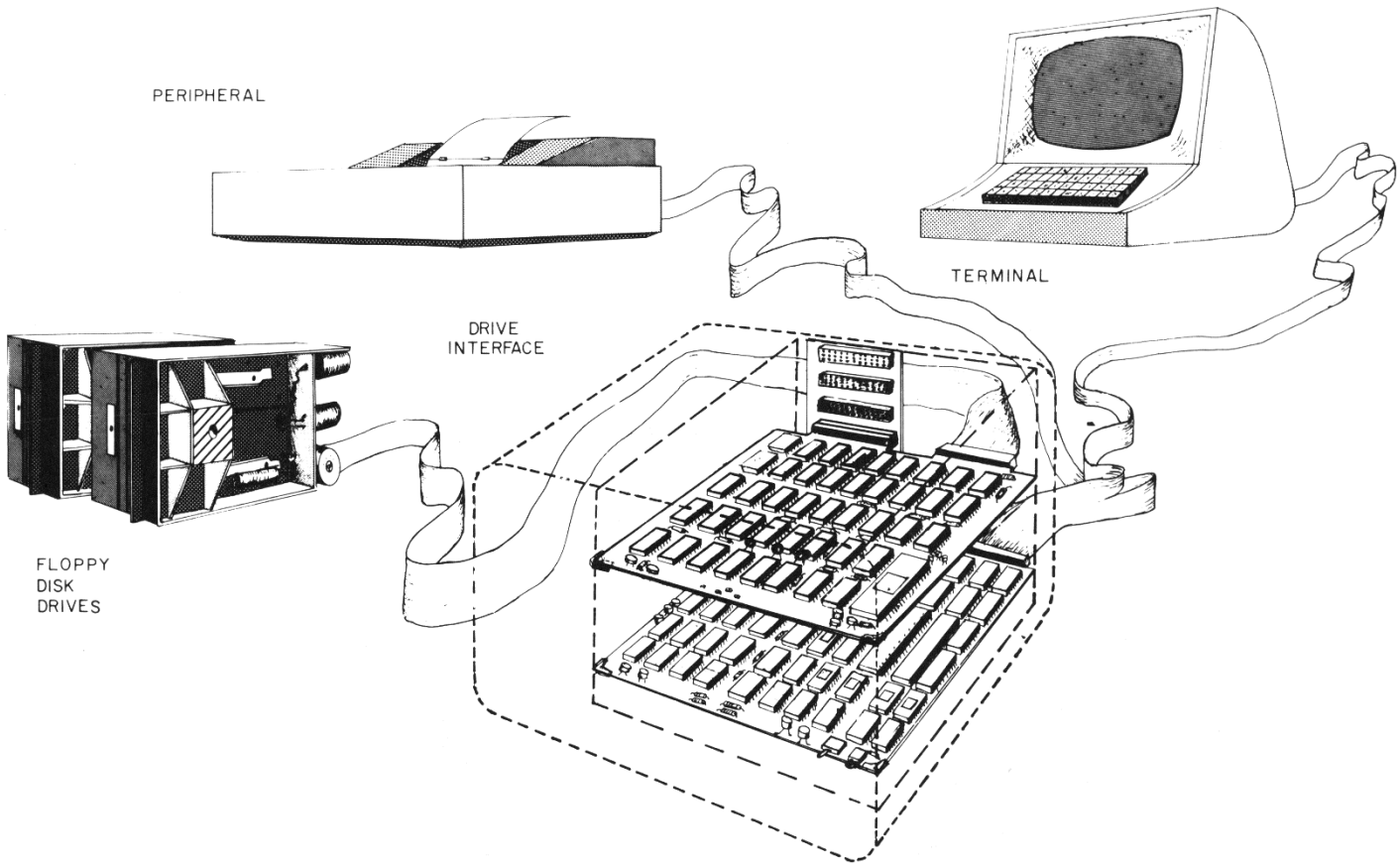
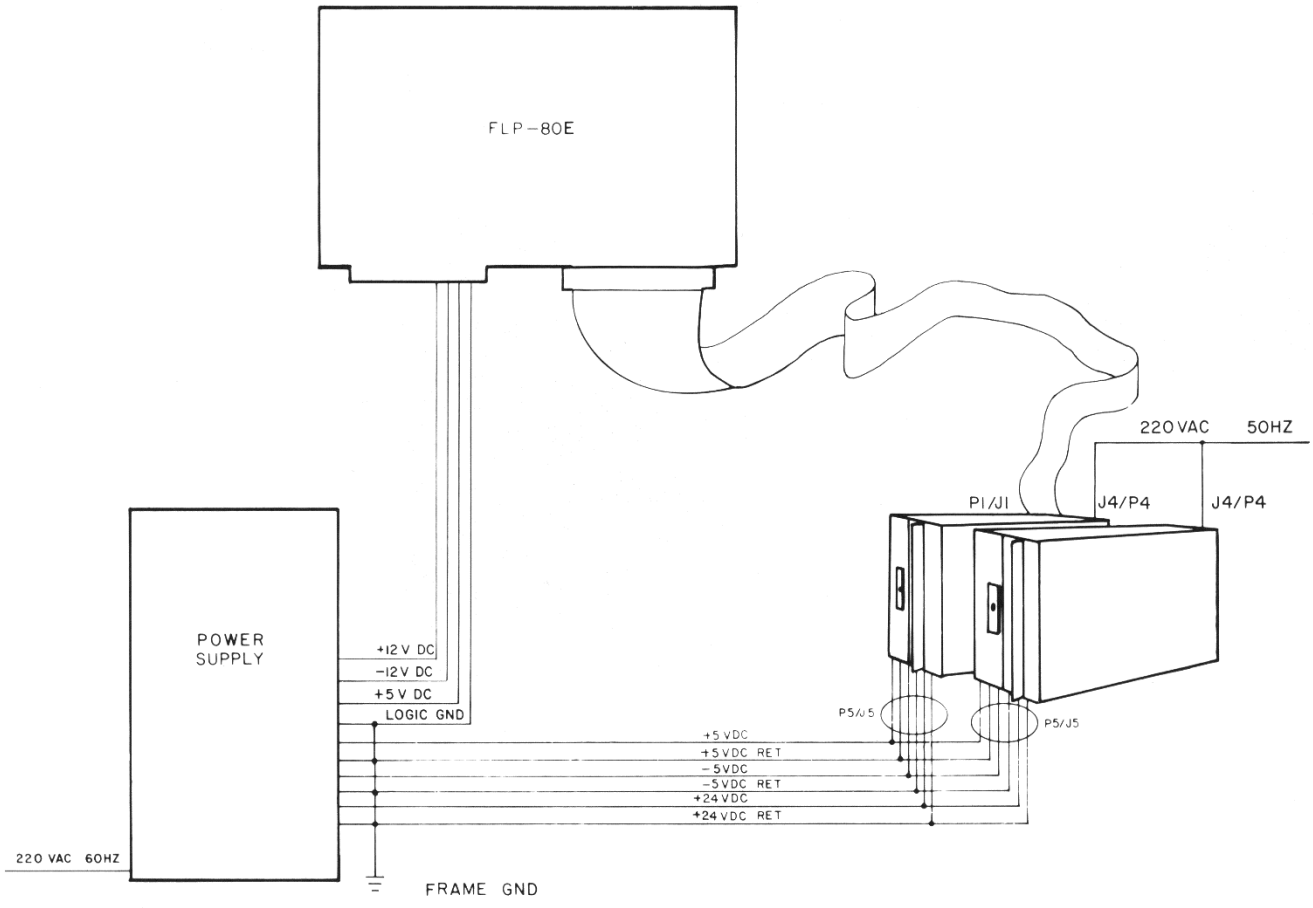


Figure 1-4. System Interconnection Diagram.



typical system configurations and required power connections.

1-15. POWER SUPPLIES. (current measured with 2 SHUGART SA800 drives connected)

Table 1-1. FLP-80E Current Requirements.

FLP-80 CONNECTOR J1	VOLTAGE	MAXIMUM CURRENT	TYPICAL CURRENT
1-4	+5V ± 5%	2.4	1.1A
91-94	+12V ± 5%	20 mA	5 mA
95,96	-12V ± 5%	64 mA	30 mA

NOTE -5V is regulated down from -12V on this card.

1-16. DRIVE POWER. The AC, DC power for the flexible disk drives is shown for a single SHUGART SA800 drive in the following tables. Refer to the SA800 or SA850 DISKETTE STORAGE DRIVE OEM manual for more details.

Table 1-2. Shugart SA800 AC Requirements.

SHUGART P4	60 Hz		50 Hz	
PIN	115 V (Standard)	208/230 V	110 V	220 V
1	85-127 VAC	170-253 VAC	85-127 VAC	170-253 VAC
2	Frame Gnd	Frame Gnd	Frame Gnd	Frame Gnd
3	85-127 Rtn	170-253 V Rtn	85-127 V Rtn	170-253 V Rtn
MAX CURRENT	0.5 Amps	0.4 Amps	0.6 Amps	0.4 Amps
FREQ TOLERANCE	±0.5 Hz		±0.5 Hz	

NOTE Assure that the proper model has been selected to correspond to input voltage requirements.

Table 1-3. Shugart SA800 DC Requirements (Each Drive)

P5 PIN	DC VOLTAGE	TOLERANCE	CURRENT	MAX RIPPLE (p to p)
1	+24 VDC	±1.2 VDC	1.7 A Max 1.3 A Typ	100 mv
2	+24 V Return			
3	- 5 V Return			
4	- 5 VDC	±0.25VDC	0.07 A Max 0.05 A Typ	50 mv
	Optional - 7 to -16 VDC (Cut Trace 'L')	NA	0.10 A Max 0.07 A Max	NA
5	+ 5 VDC	±0.25 VDC	1.0 A Max 0.8 A Typ	50 mv
6	+ 5 V Return			

Table 1-4. FLP-80E Connectors.

CONNECTOR	NO. OF PINS	MATING CONNECTOR
SK1, SK2	64	AUGAT 14--5-24P2 ELCO 00-8257-096-000-525

1-17. DC Power Connector. J5 (See Figure 1-5a) is mounted on the non-component side of the PCB and is located below the AC motor capacitor of the disk drive unit. J5 is a 6 pin AMP Mate-N-Lok connector P/N 1-380999-0. The recommended mating connector (P5) is AMP P/N 1-480270-0 utilizing AMP pins P/N 60619-1. J5 pins are labeled on the component side of the PCB with pin 5 located nearest J1/P1. Figure 1-5a illustrates J5 connector as seen on the drive PCB from non-component side.

1-18. AC Power Connector. J4, (See Figure 1-5b) is mounted on the AC motor capacitor bracket and is located just below the capacitor of the disk drive unit. J4 connector is a 3 pin connector AMP P/N 1-480305-0 with pins P/N 60620-1. The recommended mating connector (P4) is AMP P/N 1-480303-0 or 1-480304-0 both utilizing pins P/N 60619-1. Figure 1-5b illustrates J4 connector as seen from the rear of the drive.

1-19. LOGIC INTERFACE CONNECTOR. Figure 1-6 illustrates the logic cable connections between the FLP-80E board and a disk unit.

1-20. MECHANICAL DESCRIPTION.

1-21. The FLP-80E was placed on Mostek's standard size development board (250 mm x 233.4 mm). This card size is compatible with the F8 and Z80 series of development boards as well as with Mostek's "AID" development station.

1-22. All system control lines were brought to the edge connector (SK1) while all drive signals were brought to the edge connector (SK2). Signals to multiple drives are daisy chained to each drive from the drive connector. Refer to Table 1-6 for the connector pin out description.

Table 1-5. Physical Characteristics of FLP-80E Board.

Board Width	=	233.4 mm
Board Height	=	250.0 mm
Board Depth	=	1.65 cm
Weight	=	.32 kg

Figure 1-5a. SA800 J5 Connector.

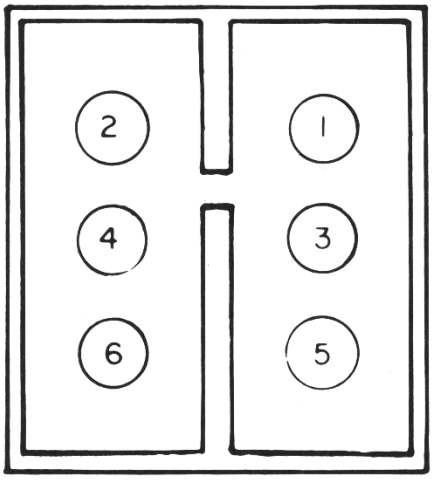


Figure 1-5b. SA800 J4 Connector.

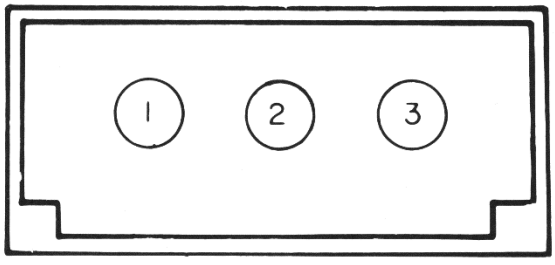


Figure 1-6. SA800 Interface Connectors.

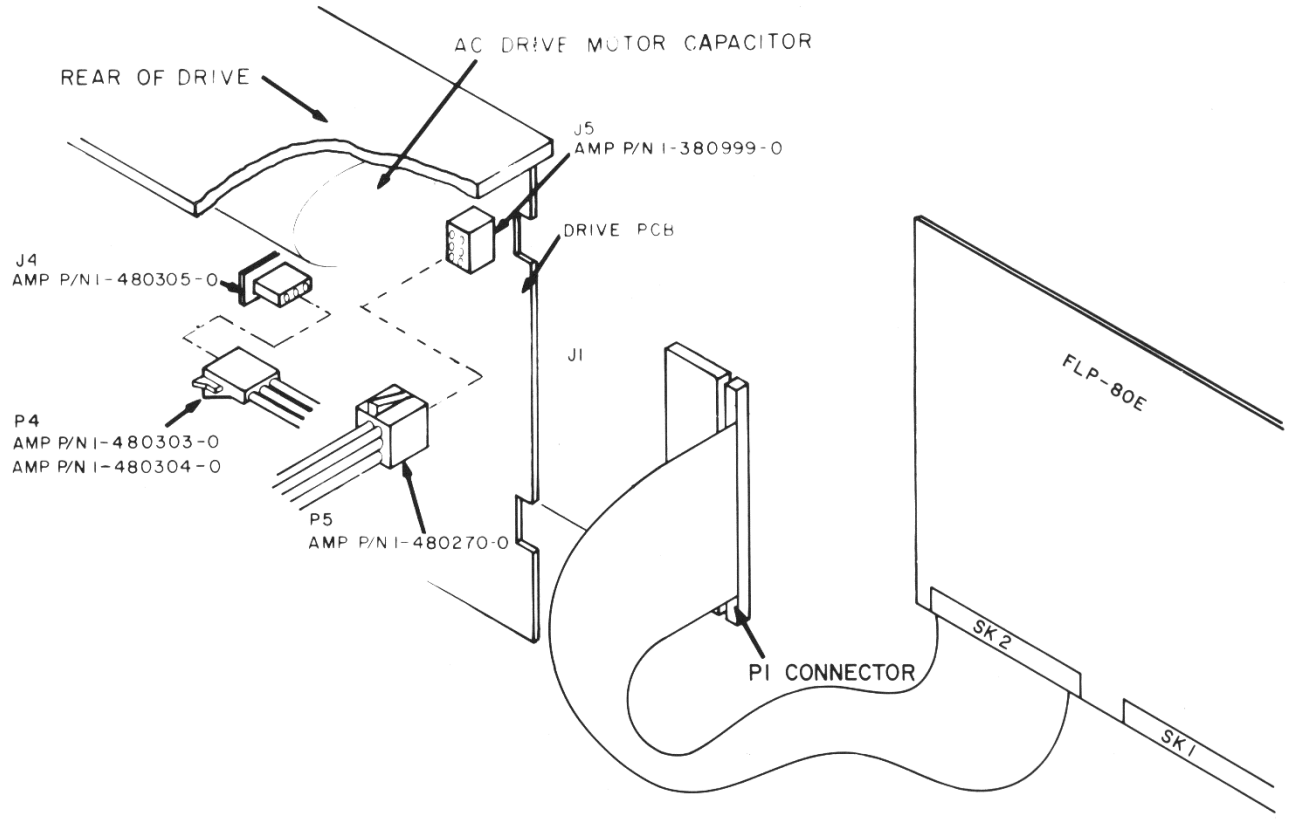


Table 1-6. FLP-80E Connector Pin Out.

SK1					
a		c	a		c
SIGNAL	PIN	SIGNAL	SIGNAL	PIN	SIGNAL
GND	1	GND	GND	1	GND
GND	2	GND	GND	2	GND
-12V	3	-12V	CK/TG3B	3	
+5V	4	+5V	XFER	4	
+5V	5	+5V	RESET	5	
+12V	6	+12V		6	
	7			7	
IEOB	8	IEIB	GND	8	
BUSAKB	9	BAI	GND	9	
	10		GND	10	RD DATA
RESETB	11		GND	11	WRT PROT
	12	MIB	GND	12	TRACK 00
	13		GND	13	WRT GATE
	14		GND	14	WRT DATA
	15		GND	15	STEP
	16	RDB	GND	16	DIRECTION
IB	17	AOB	GND	17	DRIVE SEL 4
IORQB	18	A1B	GND	18	DRIVE SEL 3
	19	A2B	GND	19	DRIVE SEL 2
	20	A3B	GND	20	DRIVE SEL 1
	21	A4B	GND	21	
DINB	22	A5B	GND	22	READY
	23	A6B	GND	23	INDEX
	24	A7B	GND	24	HLD
DOB	25		GND	25	
DIB	26		GND	26	SIDE SELECT
D2B	27		GND	27	
D3B	28		GND	28	
D4B	29		GND	29	
D5B	30		GND	30	TG43
D6B	31		GND	31	
D7B	32		GND	32	

1-23. JUMPER OPTIONS. The FLP-80E was designed to be used optionally with the dual sided disk drives, OEM applications and optional port addresses. The following list describes the Jumper conbinations possible. The Jumpers are etched in place. To initiate a change requires cutting foil, placing wire wrap posts in holes and wire wrapping new jumper.

1-24. OEM Cards.

SDB-80	OEM CARDS	USE
E5 - E7	E6 - E7	Timing chain clock
E8 - E9	E8 - E10	Invert Read Signal
E12 - E13	E11 - E13	Substitute XFER for IORQB
E15 - E16	E14 - E15	Change reset pin
E28 - E29	E27 - E29	Write/read line

1-25. Dual Sided Disks.

SINGLE SIDED	DUAL SIDED	USE
E1 - E2	OPEN	Identify dual sided

1-26. Interrupts. For use with OEM applications where the use of interrupts is required.

SDB-80E	OEM	
open	E4 - E3	Interrupts to CLK/TRG3 on SDB80E

1-27. When this Jumper is in place, interrupts which occur at the end of every operation are allowed to interrupt channel 3 of the CTC on the SDB-80. This interrupt request will be vectored by the CTC unit to interrupt the CPU.

1-28. Optional Port Addresses. For use with optional port addresses, a spare inverter U17 pin 1,2 (E1, E2) is furnished. To change port address to optional locations (see port map Figure 4-1) the foil between the following points can be cut and

a inverter installed by means of wire wrap posts and wire. Figure 1-7 shows an example of changing ports E2-E7 to Ports 62-67.

NEW PORT ADDRESSES	CUT FOIL BETWEEN	JUMPER BETWEEN
62 - 67	E18 - 15	E18-E1, E15-E2
A2 - A7	E19 - E16	E19-E1, E16-E2
C2 - C7	E20 - E17	E20-E1, E17-E2

1-29. FLP-80E SPECIFICATION SUMMARY.

COMPATIBLE CPU TYPE

Z80

WORD SIZE

Data: 8 bits

CPU/FLP-80 CLOCK FREQUENCY

2.85 MHZ MAX

2.458 MHZ (SDB80)

DATA CLOCK CRYSTAL FREQUENCY

4.00 MHZ

DATA CLOCK FREQUENCY/PERIOD

2.00 MHZ/500 ns

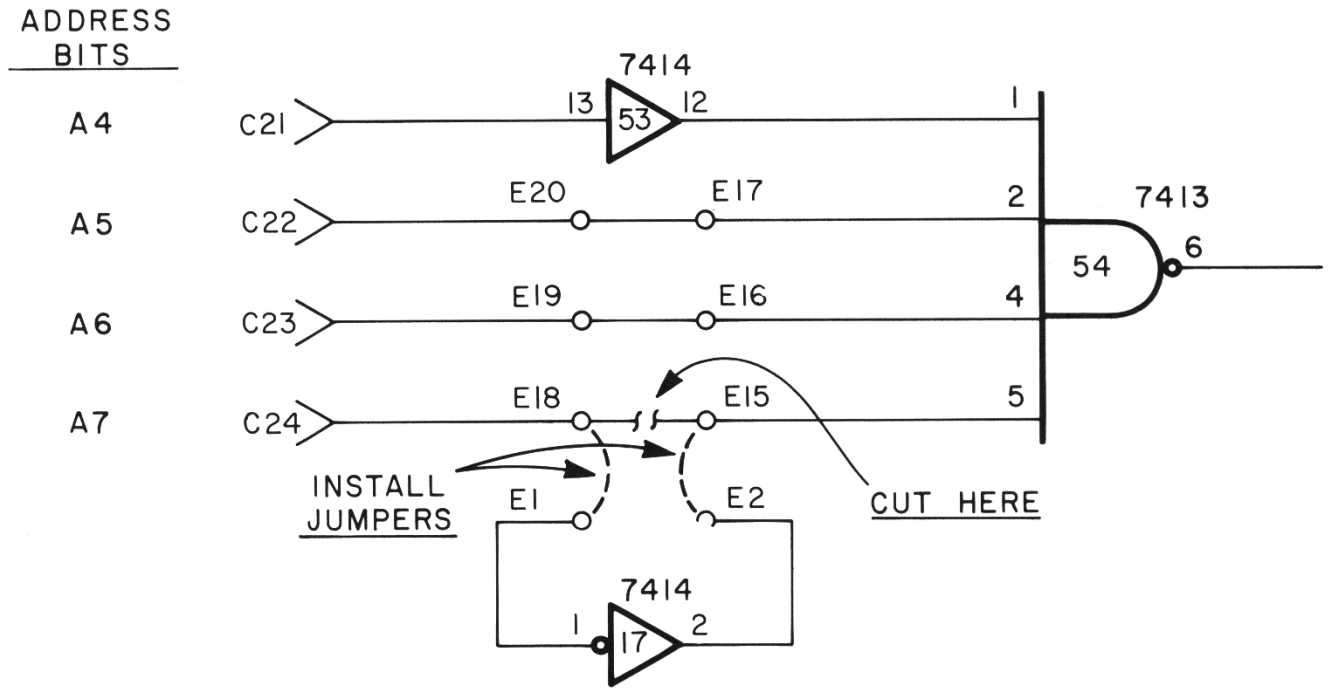
INTERRUPTS

Optional Interrupt capability as strapped option. On Mostek SDB-80E system this may interrupt channel 3 of CTC located on SDB-80E board.

PORT ADDRESSES

PORT	READ	WRITE
E2	STATUS TO CPU	
E3	CONTROL TO CPU	CONTROL FROM CPU
E4	STATUS REGISTER	COMMAND REGISTER
E5	TRACK REGISTER	TRACK REGISTER
E6	SECTOR REGISTER	SECTOR REGISTER
E7	DATA REGISTER	DATA REGISTER

Figure 1-7. Port Change Example.



EXAMPLE SHOWN FOR CHANGING PORTS E2-E7 TO PORTS 62-67

Optional strapping allows the above combination to be changed to:

62 - 67
A2 - A7
C2 - C7

INTERFACES

CPU Bus: All signals TTL Compatible

DRIVE INTERFACE Open collector TTL Output drivers capable of sinking low level output current of 48 mA. Inputs are Schmitt-trigger inputs with 150 pull up resistors.

CONNECTORS

CONNECTOR	NO. OF PINS	MATING CONNECTOR
SK1, SK2	64	AUGAT 14005-24P2 ELCO 00-8257-096-000-524

POWER SUPPLIES	MAX	TYPICAL
+ 5V ± 5%	2.4A	1.1A
+12V ± 5%	20 mA	5 mA
-12V ± 5%	64 mA	30 mA

NOTE -5V is regulated down from -12V on this card.

PHYSICAL CHARACTERISTICS

Board Width	=	233.4 mm
Board Height	=	250.0 mm
Board Depth	=	1.65 cm
Weight	=	.32 kg

SECTION 2

INSTALLATION

2-1. INTRODUCTION.

2-2. The FLP-80E board has been fully tested by MOSTEK prior to shipment. The following initial checkout procedure is simply a functional check of the board. If the board fails to perform any of the steps outlined, turn off the power, recheck the board hook up, and try the checkout procedure again. If the problem persists, contact MOSTEK for assistance.

2-3. UNPACKING.

CAUTION Some of the integrated circuits in this assembly are high impedance MOS devices. Internal circuitry is included on each device to protect the inputs against damage due to static voltage; however, the assembly should be left in the conductive bag until ready for installation.

2-4. MINIMUM EQUIPMENT NEEDED.

2-5. This check out procedure assumes the following minimum equipment availabl. For OEM applications with different CPU systems principles will still apply.

1. A serial ASCII terminal i.e. TTY, Silent 700, or CRT.
2. SDB Board
3. Power Sunplies (SDB,FLP80E, 2 drives)
   +12V @ 3A
   + 5V @ 10.0A
   -12V @ .5A
   +24V @ 3A

2-6. CONNECTIONS.

2-7. Power should be supplied to the board per the following pin out:

POWER	CONNECTOR	
+12V	J1	SK1 a6, c6
+ 5V	J1	SK1 a4, c4, a5, c5
GND	J1	Sk1 a1, c1, a2, c2
-12V	J1	SK1 a3, c3

Refer to paragraph 1-19 for description of connections.

2-8. SDB CHECKOUT.

2-9. The terminal/SDB should be connected and checked out per the manual for the SDB-80E board. The drives should be connected per paragraph 1-16 of this manual and SHUGART drive manuals.

2-10. Communication between SDB and FLP-80E can be assured by executing the following tests. Throughout this manual the following symbol convention is used:

1. ↓ indicates CARRIAGE RETURN
2. ^ indicates CARAT or UP ARROW
3. ____ underline indicates portion of command entered by user as in:
   M 5000 ↓ user entering command to display memory location 5000 followed by carriage return.
   5000 XX ↓ SDB responds with location 5000 and contents of location 5000, user enters carriage return. (XX as used here indicates current, unknown or don't care contents of memory location 5000)
4. a,b,c...u..xyz lower case letters used to indicate operands

Note that disk units may or may not be attached.

```
.P   E3↓
E3 XX FF^; Test for
E3 FF 00^; Communication
E3 00 .  ; SDB to FLP-80

.P E2^     Check Status (READ ONLY)
```

E2 XX . If XX is F8, FA, F9, It means:
F8 = Single sided, no interrupt, FIFO empty, FIFO ready
F9 = Double sided, no interrupt, FIFO empty, FIFO ready
FA = Single sided, interrupt, FIFO empty, FIFO ready

Refer: To Table 4-1 for further explanations

These are normal indications after a master clear condition (i.e. power up, switch depressed on SDB, or etc).

```
.P    E5 ↓   (Note: Port E3 must be 00.)
E5 XX FF↑
E5 FF ØØ ↑
E5 ØØ .
.P    E6 ↓
E6 XX FF↑
E6 FF ØØ
E6 ØØ .
.P E7 ↓
E7 XX FF↑
E7 FF ØØ↑
E7 ØØ .↓
```

The above three operations test communication to controller chip located within FLP-80.

2-11. If the drive or drives are connected and a diskette is inserted, the following test can be performed.

```
.P    E3 ↓
E3 XX 01↑  Select Drive 1 (02 for Drive 2)
E3 01 ↓
E4 XX 0A↑  RESTORE (seek track Ø) command*
E4 XX ↓
E5 ØØ ↓    Track register should now contain zero
E6 XX ↓
E7 XX 4C↑  Data register is loaded with desired track
E7 4C .
```

```
.P     E4 ↵
E4 04 1A/\  Head on disk unit should load and the drive should
            position to track 76.*
E4 xx 02 ↵  Head should restore to track zero.*
```

*An audible sound should be heard from the drive as it performs each task.

The above test checks the following items:

1. Selecting of a drive (Port E3)
2. Does a return to zero seek or restore.
3. Test Track Register for current position (zero after a restore).
4. Loads the data register with desired track location.
5. Does a head load and seek.

2-12. This test sets the Track Register with the current position of the Read/Write head. Then sets the desired track value into the Data Register. The controller chip will update the Track register and issue stepping pulses to the selected drive in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register at which time motion stops.

2-13. Upon successful completion of the above tests drive diagnostics may be run or operation can be attempted if no diagnostics are available.

SECTION 3

OPERATION

3-1. INTRODUCTION.

3-2. The FLP-80E will accept and execute eleven commands. Command words should be loaded in the command register when the busy status is off. Three types of commands are supported.

Type I: Head positioning, restore, seek, step, step-in, step-out.
Type II: Read or Write command
Type III: Read address, read track, write track & force interrupt

3-3. Refer to paragraph 4-36 for a discussion of these commands. All command, status, and data are transferred over the data bus to the controller chip. An active RE (refer to Figure 4-5) sets the controller chip in a read mode. An active WE sets the controller chip into a write mode.

3-4. HEAD POSITIONING.

3-5. Four commands cause position of the Read/Write head. The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step, an additional 10 milliseconds of head settling time takes place. The four programmable stepping rates ($r_1 r_0$) (refer to table 4-3) are tabulated under the Type 1 Commands description. The direction output is valid a minimum of 24 microseconds prior to the activation of the step pulse.

3-6. When a Seek, Step or Restore command is executed, an optional verification of Read/ Write head position can be performed by setting bit 2 in the command word to a logic 1. The verification operation begins at the end of the 35 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete. If track comparison is not made but the CRC checks, an interrupt is generated, the Seek Error status bit (bit 4) is set, and the Busy status bit is preset. If there is no track comparison nor a valid CRC, a step is

made in the same direction as specified and the verify operation is repeated. The additional stepping can be repeated twice to account for two defective tracks. If no verification is received at this point, the Seek Error (bit 4) is set in the Status Register.

3-7. The Head Load (HDL) output controls the movement of the Read/Write head against the diskette for data recording or retrieval. It is activated at the beginning of a Read, Write (E flag on) or Verify operation, or a Seek/Step operation with the head load bit (h) a logic high; it remains activated until the third index pulse following the last operation which uses the Read/Write head. The operation is delayed 35ms to allow engagement of the head against the diskette. In the Seek and Step commands, the head is loaded at the start of the command execution when the h bit is a logic 1. In a verify command, the head is loaded before stepping to the destination track on the diskette whenever the h bit is a logic 0.

3-8. **DISK READ OPERATION.**

3-9. On disk read operations, data is received from the disk in a serial data stream. The Data Request (DRQ) signal output is activated when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the FIFO. A (DRQ) signal and a (INRDY) Input Ready from the FIFO initiate a ($\overline{RE}$) read operation and clears the DRQ signal. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor (FIFO) readout, the lost data bit is set in the status register. The read operation continues until the end of sector is reached.

3-10. **DISK WRITE OPERATION.**

3-11. On disk write operations, the Data Request (DRQ) is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data as indicated by (OUTRDY) Output Ready from the FIFO and DRQ initiating an ($\overline{WE}$) Write signal. If new data is not loaded at the time the next serial byte is required by the flexible disk drive, a byte of zeros is written and the Lost Data bit is set in the Status Register. The Lost Data bit and certain other bits in the Status Register will activate the

Interrupt Request (INTRQ) output. The Interrupt Request signal remains activated until reset by reading the Status Register to the processor or by loading the Command Register. In addition, the INTRQ output is generated by the Force Interrupt command. After data is loaded from the processor into the Data Register, and is transferred to the Data Shift Register, data will be shifted serially through the Write Data (WD) output. Interlaced with each bit of data is a positive clock pulse of 0.5 microsecond duration.

3-12. When writing is to take place on the diskette, the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing, the first data byte must be loaded into the Data Register in response to a Data Request before the Write Gate signal can be activated.

3-13. Writing is inhibited when the Write Protect (WPRT) input is a logic 0, in which case any Write command is immediately terminated, an interrupt is generated, and the Write Protect status bit is set.

3-14. Whenever a Read or Write command is received, the Controller chip samples the Ready input. If this input is logic 0, the command is not executed and an interrupt is generated. The Seek or Step commands are performed regardless of the state of the Ready input.

THEORY OF OPERATION

4-1. INTRODUCTION.

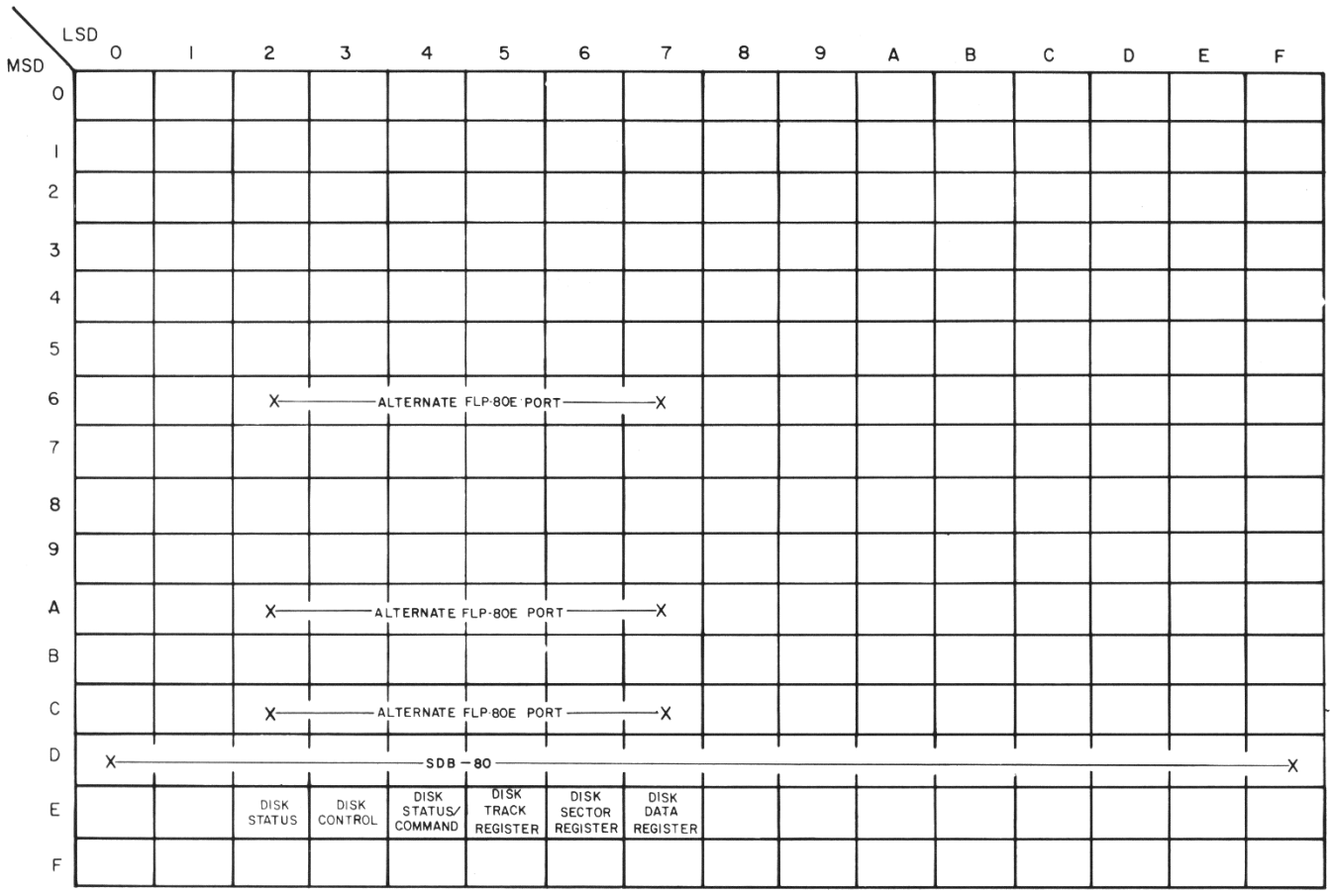
4-2. Figure 1-2 is the general block diagram of the FLP-80 board. Refering to this figure, notice the processor interface consists of a 8 bit bi-directional bus for data, status, and control word transfer. A input buffer prevents excessive loading on the processor system bus. A data switch before and after the FIFO allows a choice of paths to the controller depending on what type of data is on the bus. A direct 8 bit wide data path around the FIFO exists for use when transferring control words or status to the controller chip. A buffered 8 bit wide data path thru the FIFO is used to accomplish buffering of up to a sector or 128 bytes of data. The direct path is used for formatting when special restrictions are added to the interrupt system and software to allow dedicated CPU control. The floppy disk controller chip preforms the control/transfer of data, status, and control information to the disk unit as well as communication with the system bus.

4-3. I/O PORTS.

4-4. Figure 4-1 is the I/O port map. Ports $E2_H$ and $E3_H$ are used to control the operation of the controller board in general. Ports $E4_H$ thru $E7_H$ are used to communicate with the controller chip located on the controller board.

4-5. Port $E2_H$ is an read/input only port receiving status from the controller board. Bit Ø (refer to Table 4-1) is a zero for single sided drives and a one for double sided drive systems. While it is possible to operate up to four drives with the FLP80E controller it is not possible to mix types on one system. Thus four single sided or four double sided disks may be used in one system. Bit 1 is the interrupt line from the controller chip. Interrupt will go active at the completion or termination of any operation. Interrupt is reset when a new command is loaded into the Command Register. Bit 2 is the Output Ready line from the FIFO indicating when set that at least one byte of data is stored in the FIFO. A reset condition on this bit indicates FIFO empty. Bit 3 is the Input Ready line from the FIFO indicating when set that at least one byte of data can be loaded into the FIFO. A reset condition of this bit indicates the FIFO is full of 128 bytes.

Figure 4-1. FLP-80E Port Map.



4-6. Port $E3_H$ is an input/output port which supplies the inputs necessary for controlling the actions of the controller board. Bits Ø thru 3 are used to select the desired drive. Selecting the drive does not load the head, this action takes place just prior to the necessary operation. Bit 4 when reset is used to select the first (track 0-76) side of a two sided diskette. When this bit is set it indicates the second side (track 77-153) is selected. When Bit 5 is toggled (set-reset) the FIFO is cleared of any information. This leaves the FIFO with Input Ready set and Output Ready reset. Bit 6 selects the data path either direct (for a direct path around the FIFO) or buffered (Bit 6 - set) where data is stored into or taken from the FIFO. Bit 7 establishes the direction on the FIFO such that when set the CPU can write into the FIFO while the controller chip can read from the FIFO. When this bit is reset the CPU reads from the FIFO while the controller chip is writing into the FIFO.

4-7. Port $E4_H$ on a CPU Read operation is the Status Register of the controller chip. Refer to Table 4-4, 4-5 and 4-6 for the definitions of each bit of status. A write to this port enters the Command Register of the controller chip. Notice that it is not possible to read back the contents of the Command Register since reading port $E4_H$ gets the Status Register. A discussion of the Command Register is included in paragraph 4-32.

4-8. Port $E5_H$ Track Register, Port $E6_H$ Sector Register, Port $E7_H$ Data Register are located within the controller chip. These registers may be loaded and read on a Write or Read operation. A discussion of these registers is included in paragraph 4-23.

Table 4-1. Port Assignment Summary.

PORT ADDRESSES PORT (HEX)	READ	WRITE
E2	Status to CPU	
E3	Control to CPU	Control from CPU
E4	Status Register	Command Register
E5	Track Register	Track Register
E6	Sector Register	Sector Register
E7	Data Register	Data Register

Table 4-1. Port Assignment Summary. (Contd)

INPUT PORT $E2_H$

BIT

Ø	Double sided
1	Interrupt
2	Output Ready
3	Input Ready
4	NU
5	NU
6	NU
7	NU

INPUT/OUTPUT PORT $E3_H$

BIT

Ø	Drive 1 selected
1	Drive 2 selected
2	Drive 3 selected
3	Drive 4 selected
4	Side two select
5	FIFO Reset
6	FIFO Buffering
7	FIFO Write

INPUT PORT $E4_H$ Status Register

See Table 4-4, 4-5 and 4-6 for status information summary.

NOTE That an inverter and jumpers are available to change the port addresses. See paragraph 1-28.

4-9. INTERFACES.

4-10. PROCESSOR INTERFACE. The processor and FLP-80 interface consists of a 8 bit wide data bus, address bits A0-A7, clock and the following additional lines.

1. $\overline{RDB}$ indicates that the CPU wants to read data from memory or an I/O device.
2. $\overline{IORQB}$ indicates that the lower half of the address bus holds a valid I/O address of an I/O read or write.
3. $\overline{DINB}$ is the external bus receiver enable. This line enables the data bus receivers on the SDB Board.
4. $\overline{CLK/TRG3}$ is an optional use line allowing interrupts from the FLP-80E to interrupt the CTC timer-channel 3 on the SDB80. This line must be jumpered in as option before it appears on the processor interface connector. The standard software system supplied with the SDB-80 does not use this signal.
5. XFER is an optional signal used on OEM boards The standard jumper option E12 to E13 must be changed to E11 to E13 to make this substitution.
6. $\overline{RESETB}$ is the master clear signal generated at power-on time and by depressing the Restart switch on SDB board.
7. $\overline{RESET}$ is the optional signal used in place of RESETB when using the FLP-80E board in OEM systems. Jumper option E15 to E16 must be changed to E14 to E-5 to make this substitution.
8. $\overline{WR}$ indicates the CPU wants to write data to the memory or an I/O device.

4-11. DISK DRIVE INTERFACE. The FLP-80E disk controller can controlup to four flexible disk drives. The unit is designed to interface directly with the SHUGART SA800 or SA850 Disk Storage Drives. The FLP-80E generates all controls to position the read/write head over the desired track.

4-12. The drive interface consists of signal buses daisy chained from drive to drive with termination on the last drive. The interface driver/receiver is diagrammed in Figure 4-2. The driver is an open collector output buffer with pull up resistor on the last daisy chained drive serving as a terminator. The DRIVE SEL lines determine which flexible disk drive will respond to the bus. Jumpers on each individual drive determines the unit number configuration. A diagram showing the selection scheme is shown in Figure 4-3.

Figure 4-2. Drive Multiplexed Signals.

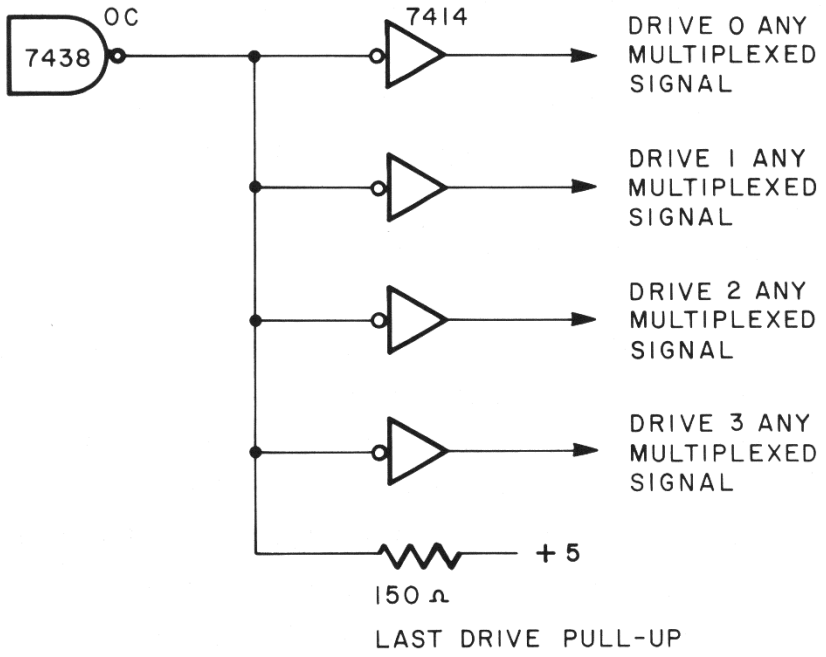
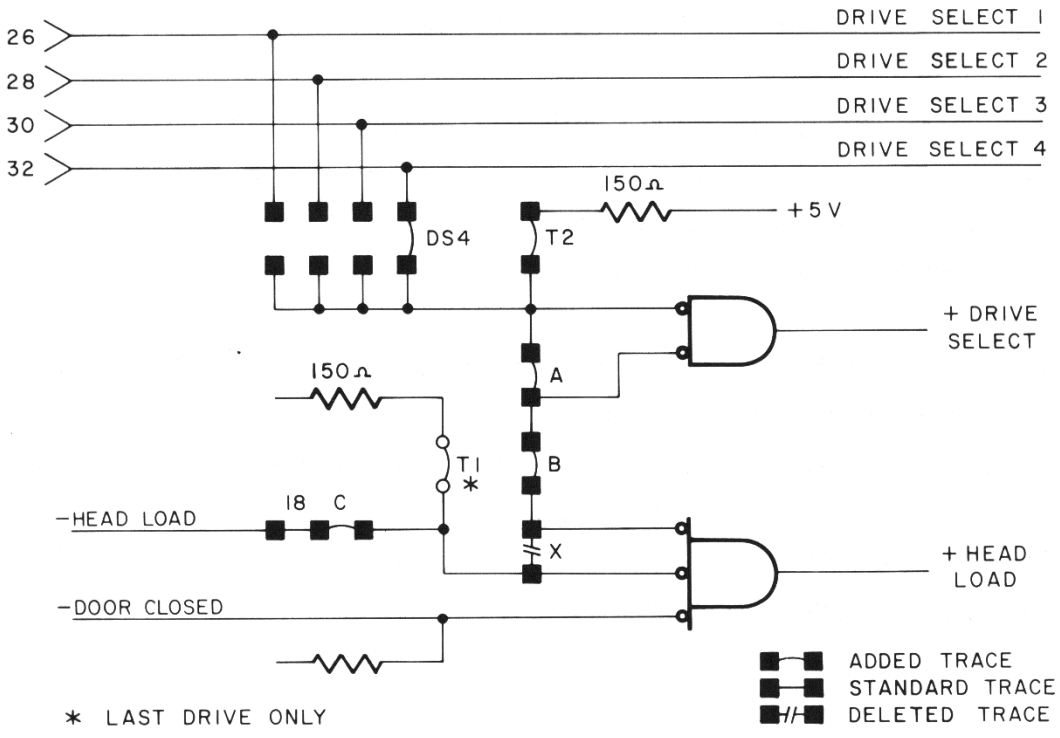


Figure 4-3. Shugart Drive Selection.



4-13. The method of motion control is by sending a level over the DIRECTION line and pulses over the STEP line to determine the motion and stepping rate for the step-direction motor within the flexible disk drive unit.

4-14. The head is loaded against the media (diskette) by the HLD (HEAD LOAD) signal. A read or write does not occur until a time out delay of 35 to 40 ms has occurred after head load. Note that the flexible disk drive does not load the head upon being selected, instead a separate head load signal (HLD) is used.

4-15. When reading serial data from the disk, the FLP-80E will look for the desired sector to be read, check its ID field and locate its data address mark. All subsequent serial data is assembled in parallel form and output thru the FIFO to the processor interface. The serial data read from the flexible diskette drive is inputed to the FLP-80E in the form of composite data in which the data and clocks are presented to the RD DATA input. A separator within the FLP-80E, separates the data and clocks then presents them separately to the controller chip.

4-16. When writing, information is presented as composite of serial clock and data pulses of 500 nsec period. With data present at the WRT DATA output, the WRT GATE signal is activated to allow write current to flow in the Read/Write head.

4-17. The remaining interface lines concern status information. The INDEX signal indicates when the index mark is encountered once per revolution. The (TR00) Track ØØ signal indicates when the Read/Write head is located over Track ØØ respectively. The (WPRT) WRITE PROTECT signal when active prevents the executing of a write command when a read only diskette is installed. The READY signal indicates the flexible drive readiness and a inactive signal prevents any read or write command from being executed.

4-18. FLEXIBLE DISK DRIVE OPTIONS.

4-19. The flexible disk drives (Example system uses SHUGART SA800 units) must be configured to the correct options for use with the FLP-80 hardware and system software. The features that should be installed in the drives used with the FLP-80 are the following:

1. Multiplexed I/O lines with up to four separate drive select lines.
2. Drive select and enable stepper without loading head option.
3. Soft Sectoring
4. Step/direction stepper motor interface.

4-20. Features which are optional to the FLP-80.

1. Track 43 sensor (low current)
2. Activity light
3. Door lock

4-21. Features not supported by FLP-80 board but found on some manufacturesdisk units.

1. WRITE FAULT indication
2. Double Track Density
3. Data Separator in drive
4. Power saver
5. Double track indication
6. Diskette type indication

4-22. The options available as straps on the SHUGART SA800 should be configured as follows for best results with the FLP-80.

1. All Drives - Y,A,B,800,DS,C,T2,L
2. Last Drive - T1,T3,T4,T5,T6
   of daisy chain
3. Drive Select - Drive Ø - DS1
   Drive 1 - DS2
   Drive 2 - DS3
   Drive 3 - DS4

Refer to Figure 4-3 of this manual, Figure 20 of SHUGART SA800 OEM MANUAL and Schematic Diagrams from SHUGART SA800 Maintenance Manual for placement of these jumpers.

4-23. FLEXIBLE DISK CONTROLLER/FORMATTER CHIP.

4-24. The FLP-80E Flexible Disk Controller Board uses a programmable floppy disk formatter/controller chip to generate the signals required to transfer data, status, and control between the CPU and disk drives. See Figure 4-4 for the pin configuration.

4.25. The Flexible Disk Controller chip block diagram is shown in Figure 4-5. The primary sections include the parallel processor interface and the Floppy Disk interface.

4.26. DATA SHIFT REGISTER. This 8-bit register assembles serial data from the Read Data input during Read operations and transfers serial data to the Write Data output during Write operations.

4-27. DATA REGISTER. This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations, the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations, information is transferred in parallel from the Data Register to the Data Shift Register. When executing the Seek command, the Data Register holds the address of the desired Track position. This register can be loaded from the Data Bus and gated onto the Data Bus under processor control.

4-28. TRACK REGISTER. This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read. The Track Register can be loaded from or transferred to the Data Bus. This Register should not be loaded when this device is busy.

4-29. AM DETECTOR. The Address Mark detector is used to detect ID, Data, and Index address marks during Read and Write operations.

4-30. TIMING AND CONTROL. All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from a 2.0 MHz crystal clock.

Figure 4-4. Controller Chip Pin Connections.

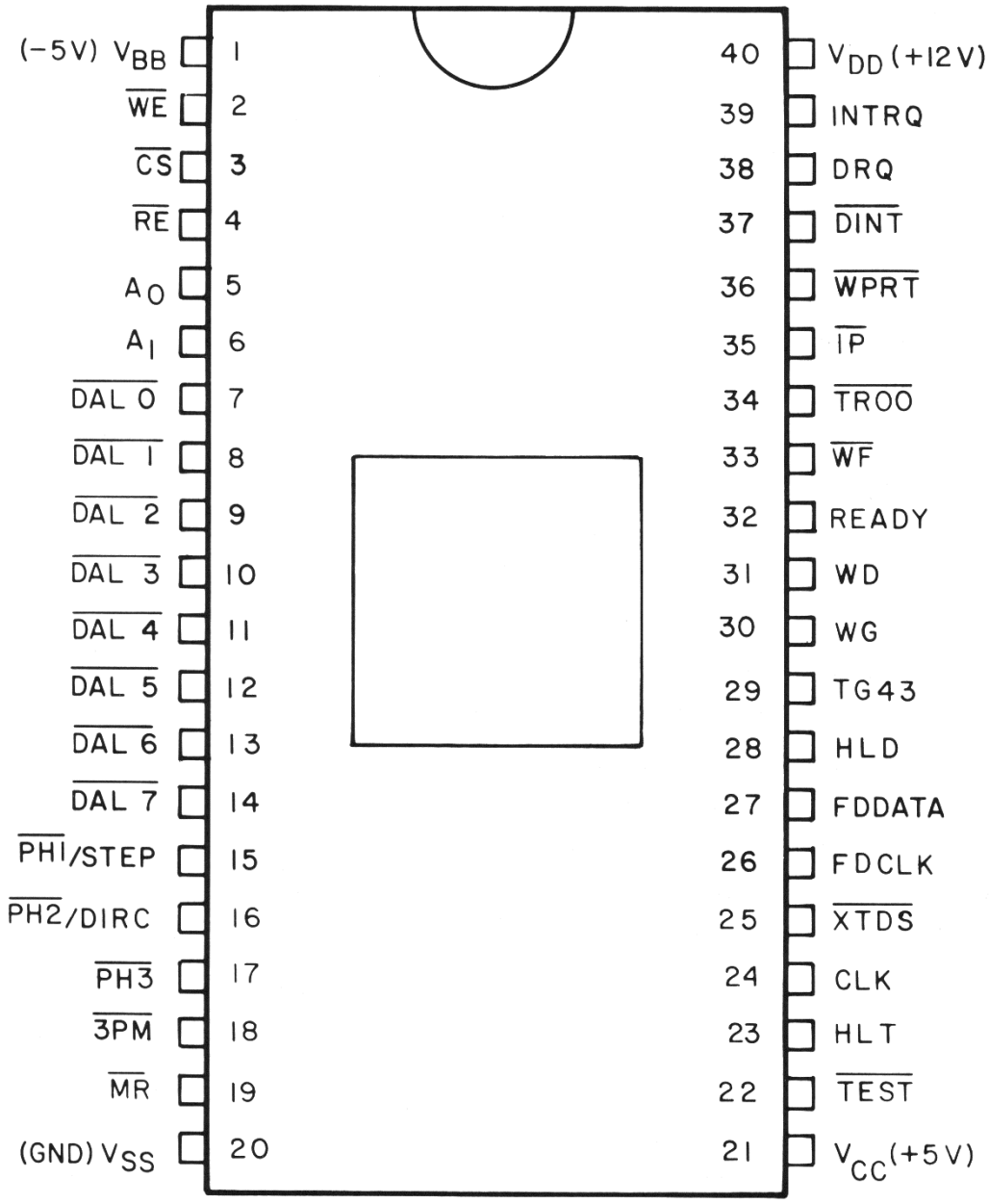
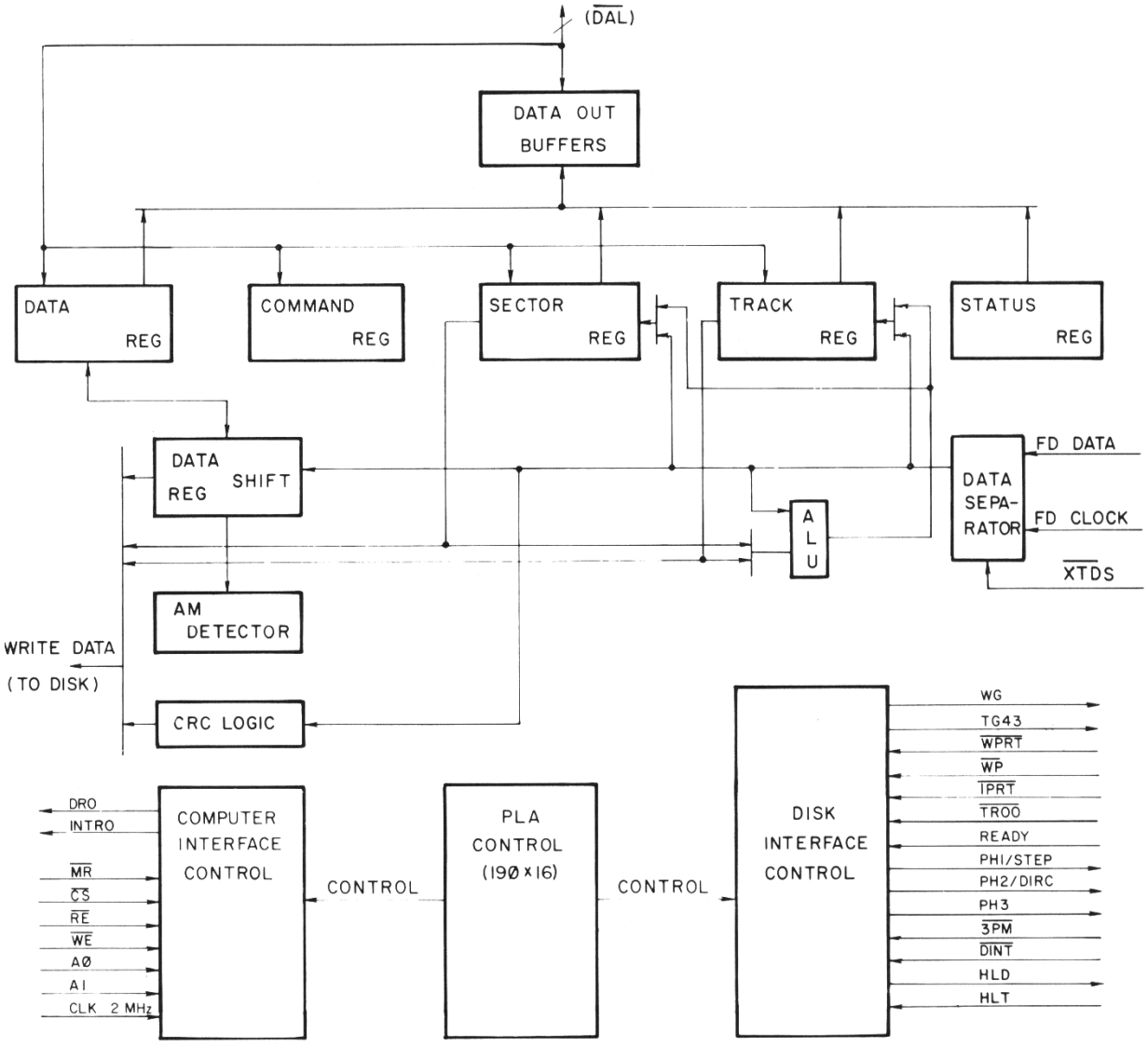


Figure 4-5. Controller Chip Block Diagram.



4-31. SECTOR REGISTER (SR). This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the Data Bus. This register should not be loaded when the device is busy.

4-32. COMMAND REGISTER (CR). This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the execution of the current command is to be overridden. This latter action results in an interrupt. The command register can be loaded from the Data Bus, but not read onto the Data Bus.

4-33. STATUS REGISTER (STR). This 8-bit register holds device Status information. The meaning of the Status bits are a function of the contents of the Command Register. This register can be read onto the Data Bus, but not loaded from the Data Bus.

4-34. CRC LOGIC. This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$. The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

4-35. ARITHMETIC/LOGIC UNIT (ALU). The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

4-36. **COMMANDS.**

4-37. The FLP-80E accepts and executes the eleven commands summarized in Table 4-2. Flags associated with these commands are summarized in Table 4-3. With the exception of the Force Interrupt command, a command word should be loaded into the internal Command Register only when bit Ø (Busy) of the Status Register is inactive (low). Whenever a command is being executed, the busy status bit is set high. When a command is completed or an error condition exists, an interrupt is generated and the Busy status bit is reset low. The Status Register indicates whether a completed command is encountered is an error or was fault free. As indicated in Table 4-2, the eleven commands accepted and executed by the FLP-80 are divided into four types. The following

paragraphs describe the eleven commands under these four divisions.

4-38. TYPE I COMMANDS. Type I Commands are basically head positioning commands and include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate (r_1r_0) field (bits 0 and 1) that determines the stepping motor rate as defined in the Table 4-2.

Table 4-2. Command Summary.

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	s
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

Table 4-3. Flag Summary.

TYPE I

h = Head Load Flag (Bit 3)

h=1, Load head at beginning

h=0, Do not load head at beginning

V = Verify flag (Bit 2)

V=1, Verify on last track

V=0, No verify

r_1r_0=Stepping motor rate (Bits 1-0)

r_1	r_0	CLK = 2 MHz TEST = 1
0	0	6 ms
0	0	6 ms
1	0	10 ms
1	1	20 ms

u = Update flag (Bit 4)

u=1, Update Track register

u=0, No update

TYPE II

m = Multiple Record flag (Bit 4)

m=0, Single Record

m=1, Multiple Records

b = Block length flag (Bit 3)

b=1, IBM format (128 to 1024 bytes)

b=0, Non-IBM format (16 to 4096 bytes)

a_1a_0= Data Address Mark (Bits 1-0)

a_1a_0=00, FB (Data Mark)

a_1a_0=01, FA (User defined)

a_1a_0=10, F9 (User defined)

TYPE III

s=Synchronize flag (Bit 0)

s=0, Synchronize to AM

s=1, Do Not Synchronize to AM

Table 4-3. Flag Summary. (Contd)

TYPE IV

Ii = Interrupt Condition flags (Bits 3-0)
- I_0=1, Not Ready to Ready Transition
- I_1=1, Ready to Not Ready Transition
- I_2=1, Index Pulse
- I_3=1, Immediate interrupt

E = Enable HLD and 10 msec Delay
- E=1, Enable HLD, HLT and 10 msec Delay
- E=0, Head is assumed Engaged and there is no 10 msec Delay.

4-39. The Type I Commands contain a head load (h) flag (bit 3) that determines whether or not the head is to be loaded at the beginning of the command. If h=1, the head is loaded at the beginning of the command (HLD output made active high). If h = 0, the HLD output is made inactive low. Once the head is loaded (HLD is active), the head will remain engaged until the FLP-80E receives a command that specifically disengages the head. If the Controller does not receive any commands after two revolutions of the disk, the head will be disengaged (HLD made inactive). The Head Load Timing (HLT) input is only sampled after a 10 millisecond delay, when actual reading or writing on the diskette is to occur. Note that a verification, described below, requires reading off the diskette.

4-40. The Type I Commands also contain a verification (V) flag (bit 2) that determines whether or not verificaiton is to take place on the last track. If V=0, no verification is performed. If V = 1, a verification is performed.

4-41. During verification, the head is loaded (HLD is active) and after an internal 10 millisecond delay, the HLT input is sampled. When the HLT input is active (high) the first encountered ID field is read off the disk. (Note that a external single shot is used to keep HLT inactive for 35 ms or greater). The track address of the ID field is then compared to the Track Register. If there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match and a valid ID CRC, an interrupt is generated, the Seek Error status bit (bit 4) is set high, and the Busy status bit is reset low. If there is not a valid CRC, the CRC Error status bit (bit 3) is set high, and the next encountered ID field is read off the disk for verification. If an ID field with a valid CRC cannot be found after two revolutions of the disk the controller terminates the operation and sends an interrupt (INTRQ) signal to the CPU.

4-42. The Step, Step-In and Step-Out commands contain an update (u) flag (bit 4). When u = 1, the Track Register is updated by one for each step. When u = 0, the Track Register is not updated.

4-43. Restore (Seek Track 0). Upon receipt of this command, the Track 00 (TR00) input is sampled. If TR00 is active low (indicating the Read/Write head is positioned over track 0), The Track Register is loaded with zeros and an interrupt is generated. If TR00 is not active low, stepping pulses at a rate specified by the r_1r_0 field

(bits 0 and 1) are issued until the TR00 input is active low. At this time, the Track Register is loaded with zeros and an interrupt is generated. If the TR00 input does not go active low after 255 stepping pulses, the controller gives up and interrupts with the Seek Error status bit set. Note that the Restore command is executed when the MR input goes from an active (low) to an inactive (high) state. A verification operation takes place of the V flag (bit 2) is set. The setting of the h flag (bit 3) allows the head to be loaded at the start of the command.

4-44. Seek. This command assumes that the Track Register contains the track number of the current position of the Read/Write head and that the Data Register contains the desired track number. The controller will update the Track Register and issue stepping pulses in the appropriate direction until the contents of the Track Register are equal to the contents of the Data Register. A verification operation takes place if the V flag (bit 2) is set. The set of the h flag (bit 3) allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

4-45. Step. Upon receipt of this command, the controller issues one stepping pulse to the floppy disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field (bits 0 and 1), a verification takes place if the V flag (bit 2) is set. If the u flag (bit 4) is set, the Track Register is updated. The setting of the h flag (bit 3) allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

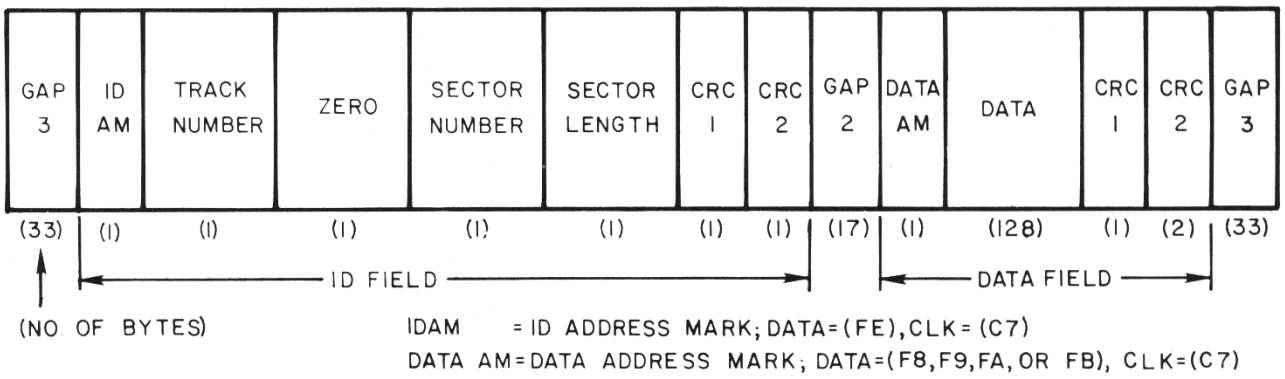
4-46. Step-In. Upon receipt of this command, the controller issues one stepping pulse in the direction towards track 76. If the u flag (bit 4) is set, the Track Register is decremented by one. After a delay determined by the r_1r_0 field (bits 0 and 1), a verification takes place if the V flag (bit 2) is set. The setting of the h flag (bit 3) allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

4-47. Step-Out. Upon receipt of this command, the controller issues one stepping pulse in the direction towards track 0. If the u flag (bit 4) is set, the Track Register is decremented by one. After a delay determined by the r_1r_0 field (bits 0 and 1), a verification takes place if the V falg (bit 2) is on. The setting of the h flag (bit 3) allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

4-48. TYPE II COMMANDS. The Type II Commands include the Read sector(s) and Write sector(s) commands. Prior to loading the Type II Commands into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II Commands, the Busy status bit is set. If the E flag (bit 2) = 1 (this is the normal case), HLD is made active and HLT is sampled after an internal 10 millisecond delay. If the E flag = 0, the head is assumed engaged and there is no internal 10 millisecond delay.

4-49. When an ID field (see Figure 4-6) is located on the diskette, the controller compares the Track Number of the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is made. If there is a match, the sector number of the ID field is then compared with the Sector Register. if there is not a match, the next encountered ID field is read and a comparison is

Figure 4-6. IBM 3740 ID Field and Data Field Formats.



made. If there is a match, the CRC field is read. (The polynomial for the CRC is $G(x) = x^{16} + x^{12} + x^5 + 1$. The CRC includes all the information starting with the address mark and up to the CRC characters.) If there is a CRC error, the CRC Error status bit is set and the next ID field is read off the diskette and comparisons are made. If the CRC is correct, the data field is located and will be either written or read, depending upon command. The controller must find an ID field with a valid track number, sector number, and CRC within two revolutions of the disk otherwise, the Record Not Found status bit (bit 4) is set and the command is terminated with an interrupt.

4-50. Each of the Type II Commands contains a (b) flag (bit 3), which in conjunction with the sector length field contents of the ID, determines the length (number of characters) of the data field. For IBM 3740 compatibility, the b flag (bit 3) should equal 1. The numbers of bytes in the data field (sector) is then 128×2^n where n = 0, 1, 2, or 3.

For b = 1:

SECTOR LENGTH FIELD (HEX)	NUMBER OF BYTES IN SECTOR (DECIMAL)
00	128
01	256
02	512
03	1024

When the b flag (bit 3) equals zero, the sector length field (n) multiplied by 16 determines the number of bytes in the sector or data field as shown below:

For b = 0:

SECTOR LENGTH FIELD (HEX)	NUMBER OF BYTES IN SECTOR (DECIMAL)
01	16
02	32
03	48
04	64
.	.
.	.
.	.
FF	4080
00	4096

4-51. Each of the Type II Commands also contains an m flag (bit 4) that determines whether multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the Sector Register internally updated so that an address verification can occur on the next record. The controller continues to read or write multiple records and update the Sector Register internally updated so that an address verification can occur on the next record. The controller continues to read or write mutiple records and update the Sector Register until the Sector Register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register. When either of these occurs, the command is terminated and an interrupt is generated.

4-52. Read Command. Upon receipt of this command, the Read/Write head is loaded and the Busy status bit is set. Then when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is inputted to the computer. The Data Address Mark of the data field must be found within 28 bytes of the correct ID field. If not, the Record Not Found status bit is set and the operation is terminated. When the first character or byte of the data field has been shifted through the Data Shift Register, it is transferred to the Data Register and a Data Request (DRQ) output is generated. When the next byte is loaded into the Data Shift Register, it is transferred to the Data Register and another DRQ output is generated, provided that the CPU has previously read the Data Register. If one or more characters are lost, the Lost Data status bit is set. This sequence continues until the data field has been inputted to the computer. If there is a CRC error in the data field, the CRC Error status bit is set, and the command is terminated (even if it is a multiple record command). At the end of the operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (bits 5 and 6) as shown below:

STATUS BIT 5	STATUS BIT 6	DATA AM (HEX)
0	0	FB
0	1	FA
1	0	F9
1	1	F8

4-53. Write Command. Upon receipt of this command, the Read/Write head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number and correct CRC, a DRQ output is generated. The controller counts off 11 bytes from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the Data Register has been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of all Zero levels are then written on the diskette. At this time, the Data Address Mark is then written on the diskette, as determined by the a_1a_0 field (bits 0 and 1) of the command as shown below:

a_1	a_0	DATA MARK (HEX)	CLOCK MARK (HEX)
0	0	FB	C7
0	1	FA	C7
1	0	F9	C7
1	1	F8	C7

The controller then writes the data field by generating DRQ outputs to the computer. If the DRQ is not serviced in time, the Lost Data status bit is set and a byte of zeros is written on the diskette. The command is not terminated. After the last byte has been written on the diskette followed by one byte of all One levels. WG is then made inactive.

4-54. TYPE III COMMANDS.

4-55. Read Address. Upon receipt of this command, the head is loaded and the Busy status bit is set. The next encountered ID filed is then read in off the diskette, and the six data bytes of the ID field are assembled and transferred to the Data Register, and a DRQ output is generated for each byte. (The six bytes of the ID field are shown in Figure 4-6)

4-56. Although the CRC characters are inputted to the computer, the controller checks for validity and the CRC Error status bit is set if there is a CRC error. The Sector Address of the ID field is written into the Sector Register. At the end of the operation, an interrupt is generated and the Busy status is reset.

4-57. Read Track. Upon receipt of this command, the head is loaded and the Busy status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled, it is transferred to the Data Register and the Data Request (DRQ) output is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. If the s flag (bit 0) of the command is low, the accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated.

4-58. The controller handles single density frequency modulated (FM) data. Refer to Figure 4-7 and 4-8. Each data cell is defined by clock pulses. A pulse recorded between clock pulses indicates the presence of a logic 1 bit; the absence of this pulse is interpreted as a logic 0 bit. The Address Marks for Index, ID, and Data are identified by a particular pattern not repeated in the remainder of the ID field or Data field. This is accomplished by reading patterns that are recorded with missing clock bits (logic 0) as shown below:

For initialization:

Write 2 CRC Characters	Data	1 1 1 1 0 1 1 1 = F7
	Clock	1 1 1 1 1 1 1 1 = FF
Index Address Mark	Data	1 1 1 1 1 1 0 0 = FC
	Clock	1 1 0 1 0 1 1 1 = D7
ID Address Mark	Data	1 1 1 1 1 1 1 0 = FE
	Clock	1 1 0 0 0 1 1 1 = C7
Data Address Mark	Data	1 1 1 1 1 0 1 1 = F9 - FB
	Clock	1 1 0 0 0 1 1 1 = C7
Deleted	Data	1 1 1 1 1 0 0 0 = F8
Data Address Mark	Clock	1 1 0 0 0 1 1 1 = C7
Spare	Data	1 1 1 1 1 1 0 1 = FD
	Clock	(user designated)

4-59. These patterns are used as synchronization code by the controller when reading data and are recorded by the formatting command (Write Track) when the controller is presented with data F7 through FE.

Figure 4-7. Data Pattern.

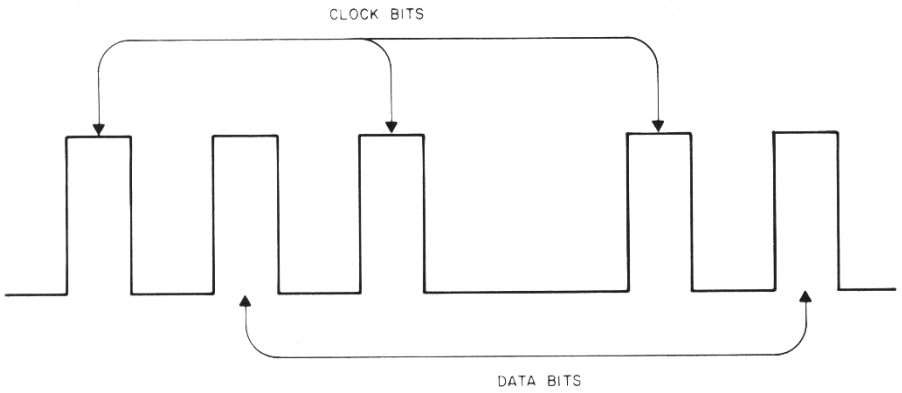
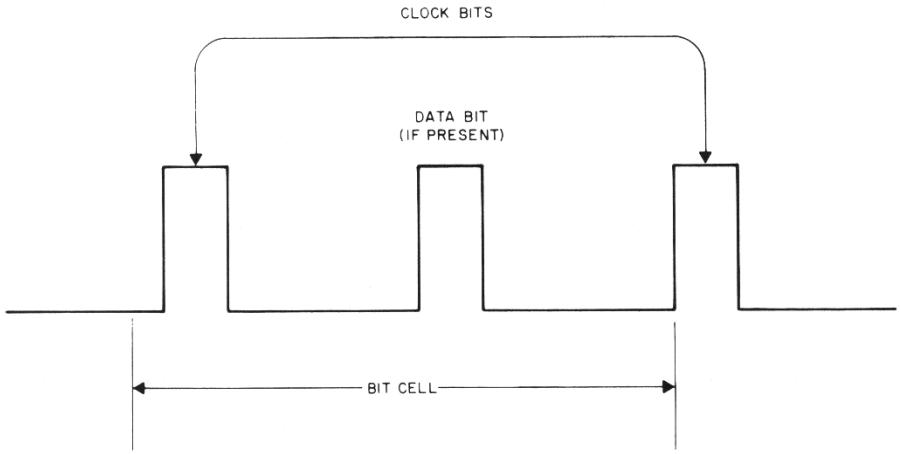


Figure 4-8. Bit Cell Definition.



4-60. Write Track. Upon receipt of this command, the head is loaded and the Busy status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request output is activated immediately upon receiving the command and writing does not start until after the first byte has been loaded into the Data Register. If the Data Register has not been loaded by the second index pulse, the operation is termianted. This sets the Not Busy and Lost Data status bits, and activates the interrupt. If a byte is not present in the Data Register when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the diskette by detecting certain data byte patterns in the outgoing data stream as shown above. The CRC generator is initialized to all Ones when any data byte from F8 to FE is about to be transferred from the Data Register to the Data Shift Register.

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN (HEX)	INTERPRETATION	CLOCK MARK (HEX)
F7	Write CRC Char.	FF
F8	Data Addr. Mark	C7
F9	Data Addr. Mark	C7
FA	Data Addr. Mark	C7
FB	Data Addr. Mark	C7
FC	Index Addr. Mark	D7
FD	Spare	
FE	ID Addr. Mark	C7

The Write Track command does not execute if the DINT input is grounded. Instead, the Write Protect status bit is set and the interrupt is activated. One F7 pattern in the Data Register generates 2 CRC characters.

4-61. TYPE IV COMMANDS. The force interrupt command can be loaded into the Command Register at any time. If there is a current command under execution (Busy status bit is set), the command is terminated and an interrupt is generated when the condition specified in the I_0 through I_3 field (bits 0 through 3) is detected. More than one condition

may be specified. The interrupt conditions are indicated below:

I_0 = Not Ready-to-Ready Transition
I_1 = Ready-to-Ready Transition
I_2 = Every Index Pulse
I_3 = Interrupt occurs within 1 to 10 milliseconds and every10 milliseconds thereafter.

NOTE If IO through I_3 = 0, no interrupt is generated; however, the current command is terminated and the Busy status bit is reset.

4-62. STATUS REGISTER.

4-63. An 8 bit register is provided in the controller to hold device status information. The status varies according to the type of command executed last. Table 4-4,4-5 and Table 4-6 summarize the information which can be read into the data bus by a read operation.

Table 4-4. Status Register Summary

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
6	WRITE PROTECT	0	RECORD TYPE	0	WRITE PROTECT	WRITE PROTECT
5	HEAD ENGAGED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	0	RECORD NOT FOUND	0
3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

Table 4-5. Status for Type I Commands.

BIT	NAME	MEANING
7	Not Ready	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the READY input and logically 'ored' with MR.
6	PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
5	HEAD LOADED	When set, it indicates the head is loaded and engaged. The bit is a logical "and" of HLD and HLT signals.
4	SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
3	CRC ERROR	When set, there was one or more CRC errors encountered on an unsuccessful track verification operation. This bit is reset to 0 when updated.
2	Track 00	When set, indicates Read Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TR00}}$ input.
1	INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
0	BUSY	When set command is in progress. When reset no command is in progress.

Table 4-6. Status Bits for Type II and III Commands.

BIT	NAME	MEANING
7	NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the READY input and 'ored' with MR. The TYPE II and III Commands will not execute unless the drive is ready.
6	RECORD TYPE/ WRITE PROTECT	On Read Record: It indicates the MSB of record-type code from data field address mark. On Read Track: Not Used. On any Write Track: It indicates a Write Fault. This bit is reset when updated.
5	RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the LSB of record-type code from data field address mark. On Read Track: Not Used. On any Write Track: It indicates a Write Fault. This bit is reset when updated.
4	RECORD NOT FOUND	When set, it indicates that the desired track and sector were not found. This bit is reset when updated.
3	CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
2	LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
1	DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
0	BUSY	When set, command is under execution. When reset, no command is under execution.

4-64. **DATA PATH DESCRIPTION.**

4-65. The processor/FLP-80E interface is a 8 bit wide data byte with the direction of data flow determined by the (RDB) Read line and (WRB) Write line from the processor, gated by (IORQB) I/O Request. This eight bit width byte may be buffered in parallel through the FIFO or presented directly to the controller chip unbuffered depending on the control lines

4-66. The controller chip changes the data to single density frequency modulated (FM) data, i.e. each data bit recorded has an associated clock bit associated with it. This information is sent to the flexible drive over the WRT DATA line on a write operation. On a read operation the data is received from the selected drive over the RD DATA line.

4-67. On a write operation, a byte of data is converted to serial data by the controller, then transferred to the disc drive with bit Ø first and bit 7 being transferred last.

4-68. On a read operation, bit Ø of each byte is transferred first with bit 7 last.

4-69. Read data entering the FLP-80E controller is separated into clocks and data by the separator circuit and presented to the controller chip on pin 27 (FDDATA) and pin 26 (FDCLK) (Refer to Figure 4-4). Note that it is not required that the separator circuit distinguish between presenting data or clocks to respective pins as long as a separation is made.

4-70. **FORMATTING THE DISKETTE.**

4-71. Formatting the disk (See Figure 4-6) is accomplished by first building a track image in memory, positioning the head over the desired track, issuing a write track command and transferring the image to the desired track. The track image consists of the following format (sent to controller) for use with IBM format of 128 bytes/sector:

	NUMBER OF BYTES		HEX VALUE OF BYTE WRITTEN
	40		00 or FF
	6	Gap	00
	1		FC (Index Mark)
	26		00 or FF
*1	6		00
Each	1	ID	FE (ID Address Mark)
Sector	1	Field	Track Number
	1		00
	1		Sector Number (1 thru 1A)
	1		00
	1		F7 (2 CRC's written by Controller Chip. See paragraph 4-61)
	11		00 or FF
	6		00
	1	Data	FB (Data Address Mark)
	128	Field	Data (IBM uses E5)
	1		F7 (2 CRC's written by controller chip. See paragraph 4-61)
	27		00 or FF
	247**		00 or FF

* Write bracketed field 26 times

** The length may vary due to track length tolerances.

4-72. The Writing sequence continues from one index mark to the next index mark. Normally whatever data pattern appears in the Data Register is written on the disk with a clock mark of $(FF)_{16}$. However, if the controller detects a data pattern of F7 thru FE in the Data Register, this is interpreted as data address marks with missing clocks or CRC generation. For instance an FE pattern will be interpreted as an ID address mark (DATA FE, CLK C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters. As a consequence, the patterns F7 thru FE must not appear in the gaps, data fields, or ID fields. When using the Write Track command.

SECTION 5

MAINTENANCE

5-1. INTRODUCTION.

5-2. The FLP-80E board requires no maintenance. The disk drives require occasional maintenance/adjustment. Refer to the drive maintenance manual for details.

5-3. TROUBLESHOOTING.

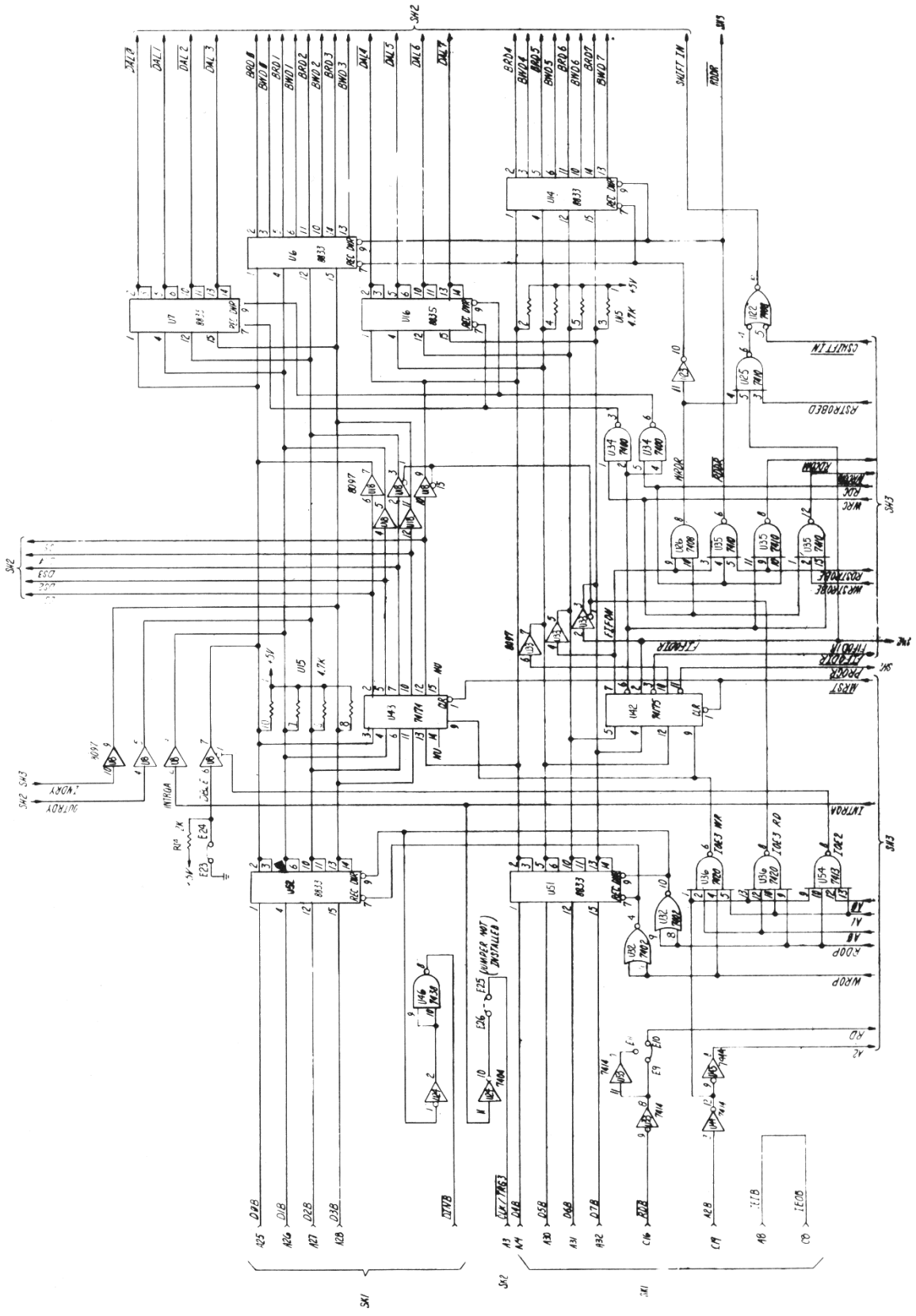
5-4. In case of troubles which have been localized to the FLP-80E board, executing the tests described in the initial checkout procedure should be helpful to trace most problems. Diagnostics may also be used to pin-point errors. If troubleshooting localizes the failure to accessing of a port or wrong data from a port, a simple program can be written to read or write to that port while troubleshooting with an oscilloscope.

5-5. Data errors can usually be found with the diagnostic programs and may be traced to FLP-80E or disk drive, or diskette media.

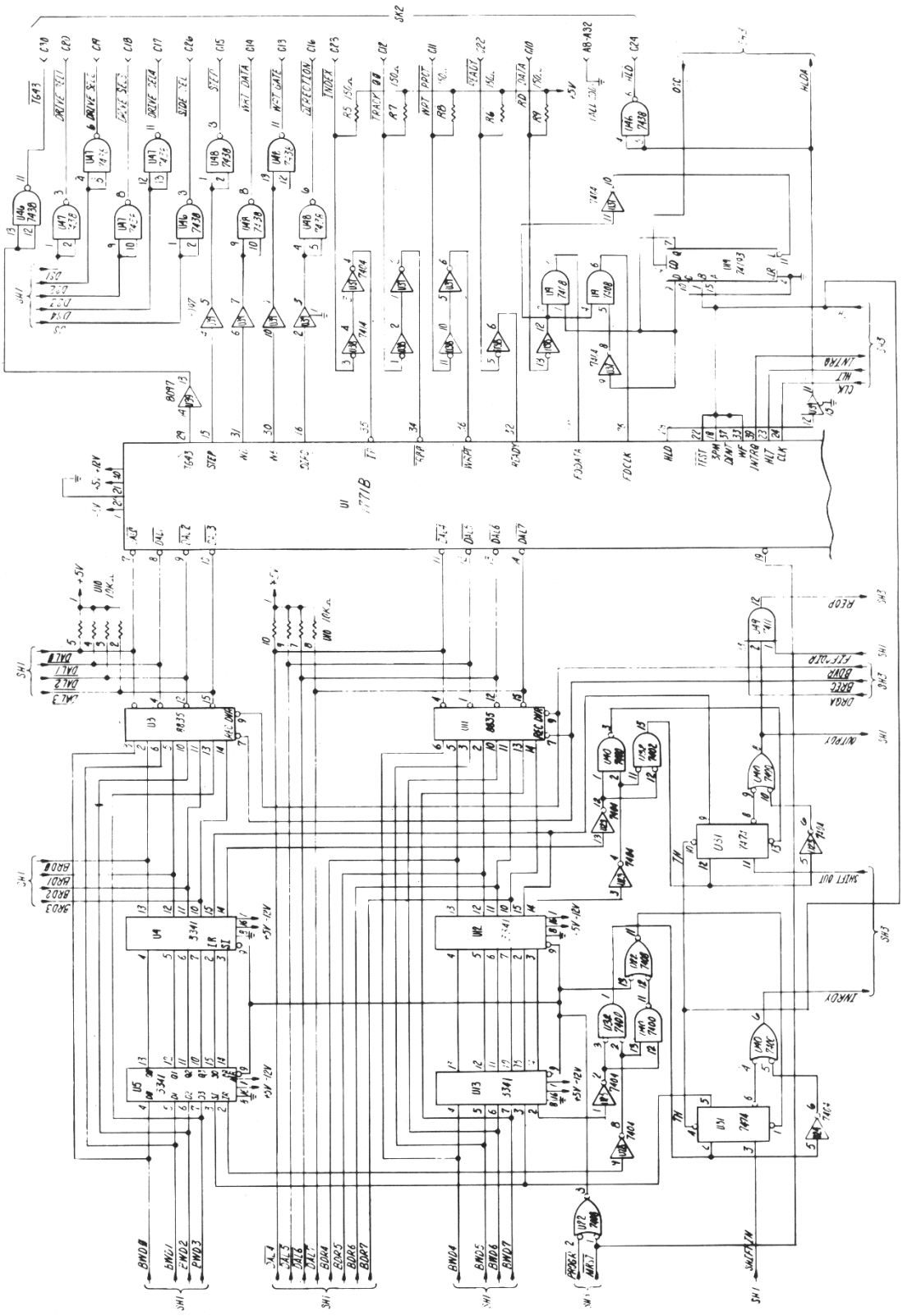
APPENDIX A

SCHEMATIC DIAGRAMS

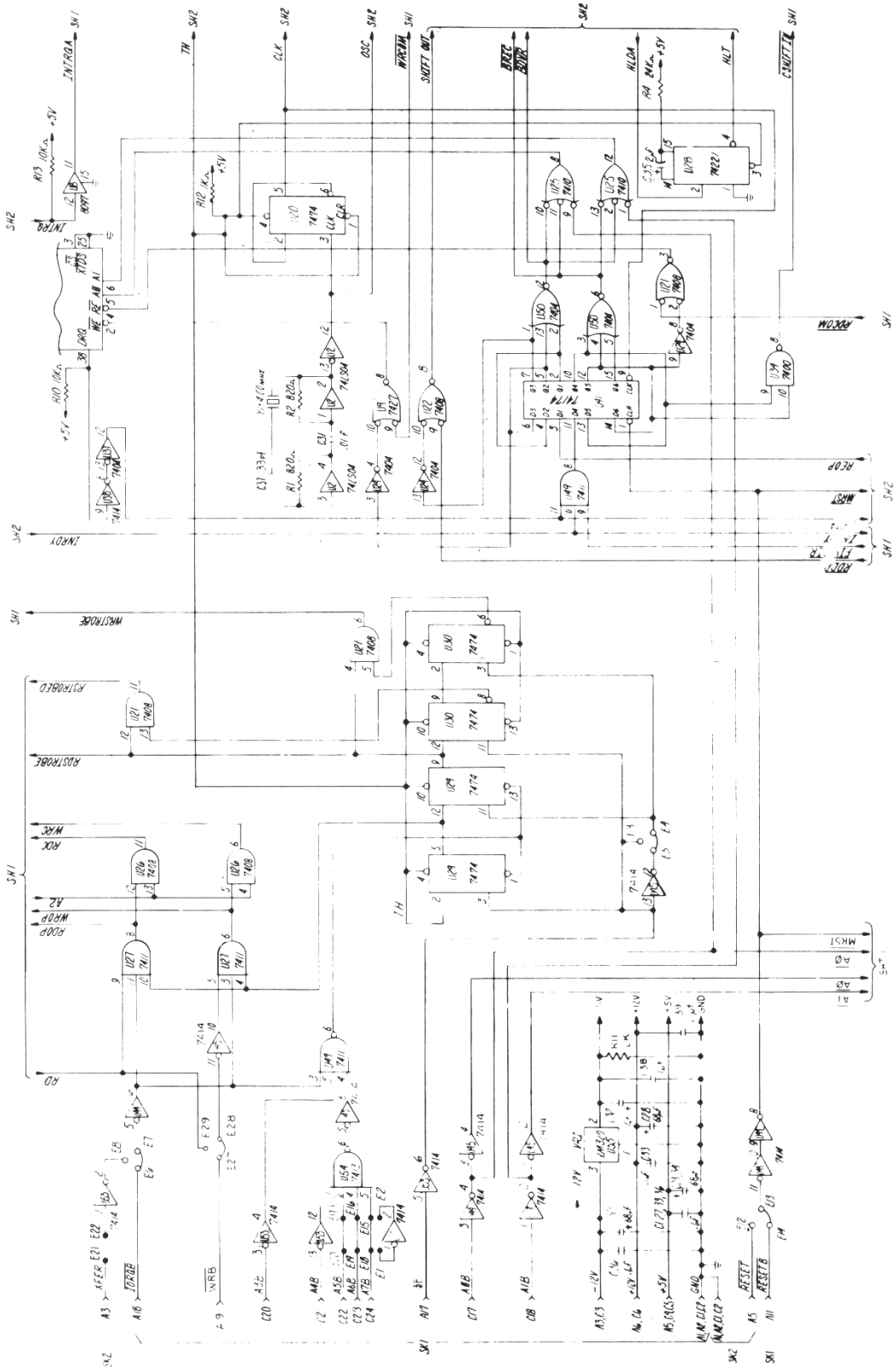
Schematic Diagram (Sheet 1).



Schematic Diagram (Sheet 2).



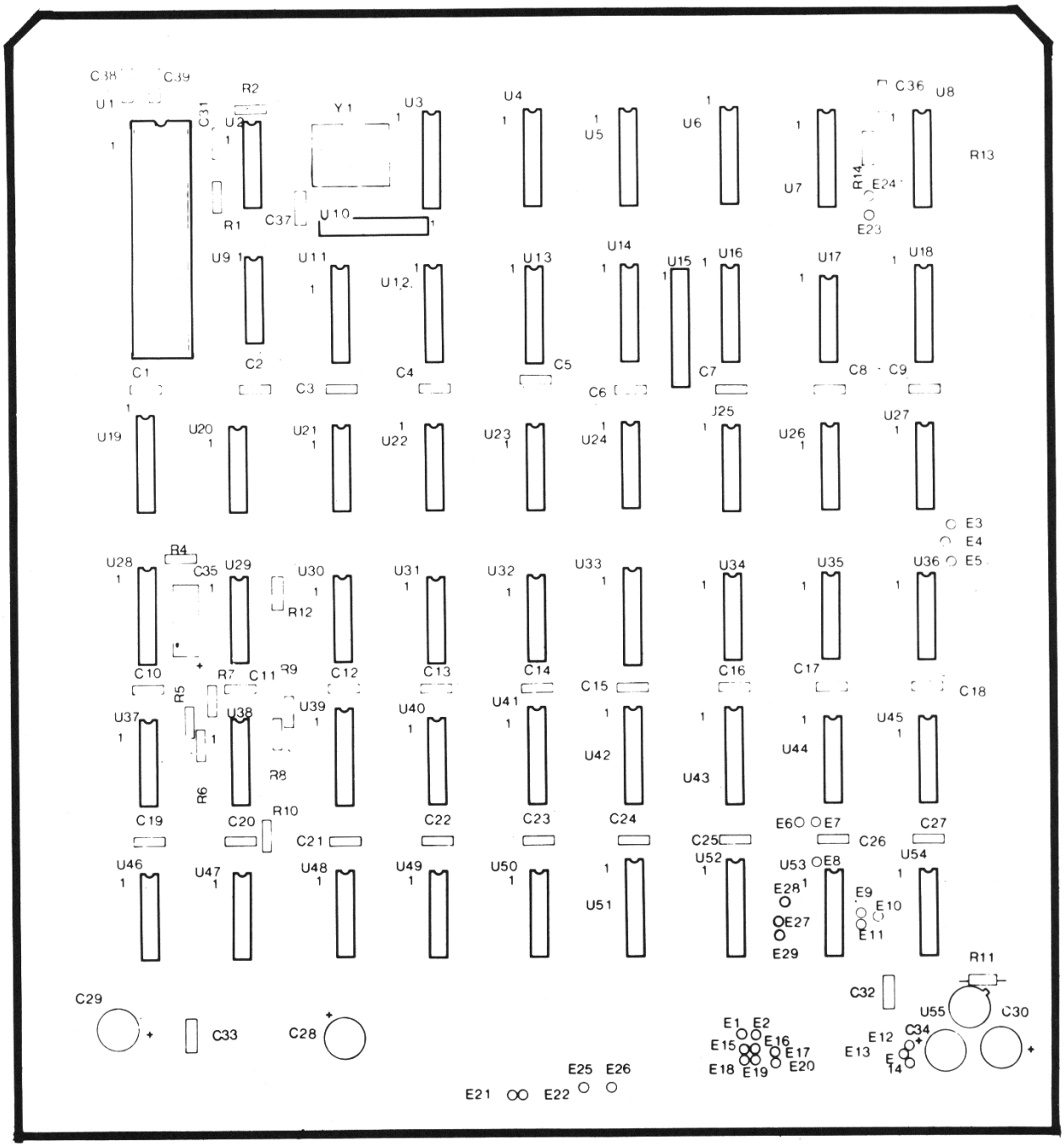
Schematic Diagram (Sheet 3).



APPENDIX B

PARTS

Parts Placement Diagram.



Parts List.

ITEM	QTY.	PART NO.	DESCRIPTION	REF. DESIG.	NOTES
43	2	4210057	CONNECTOR	SK1, SK2	
42	2	4140003	EJECTOR		
41	1	4620019	IC SOCKET 40 PIN		
40	4	4150114	CAPACITOR 68	C28,29,30,34	
39	31	4150111	0.1µf	C1-27,33, 36,38,39	
38	1	4150078	1µf	C32	
37	1	4150144	2µf	C35	
36	1	4150107	.01µf	C31	
35	1	4150086	CAPACITOR 33pf	C37	
34	1	423009	CRYSTAL 4.000 MHZ	Y1	
33	1	4470202	RES SIP 4.7K 10 PIN	U15	
32		4470200	RES SIP 10K 10 PIN	U10	
31	2	4470080	RESISTOR 2K 1/4W 5%	R11, 14	
30	1	4470073	1K	R12	
29	2	4470097	10K	R10,13	
28	2	4470071	820Ω	R1, 2	
27	5	4470053	150Ω	R5,6,7,8,9	
26	1	4470106	RESISTOR 24K 1/4W 5%	R4	
25	3	4313078	IC, 7438	U46,47,48	
24	1	4313288	74LS04	U2	
23	1	4313223	LM320H-5.0	U55	
22	1	4313016	7427	U50	
21	5	4313170	7414	U17,38,44, 45,53	
20	1	4313071	7413	U54	
19	2	4313208	7411	U27, 49	
8	2	4313012	7410	U25, 35	
7	1	4313220	74221	U28	
16	1	4313050	74193	U19	
15	4	4313032	7474	U20,29,30,31	
14	3	4313006	7404	U23,24,37	
13	1	4313004	7402	U32	
12	2	4313002	7400	U34,40	
11	4	4313010	7408	U9,21,22,26	
10	1	4313014	7420	U36	
9	4	4313154	DM8097	U8,18,33,39	
8	1	4313075	74175	U42	
7	2	4313118	74174	U41, 43	
6	1	4313420	1771B-01	U1	
5	4	4313438	3341A	U4,5,12,13	
4	4	4313408	DM8835	U3,7,11,16	
3	4	4313262	IC, DM8833	U6,14,51,52	
2	REF	450-00263-00	P.C. BD 450-00262-00		
1	REF	450-00264-00	SCHEMATIC		

B-1. FACTORY REPAIR.

B-2. In the event that difficulty is encountered with this unit, it may be returned directly to MOSTEK for repair. This service will be provided free of charge if the unit is returned within 90 days of purchase. However, units which have been modified or abused in any way either will not be accepted for service or will be repaired at the owner's expense.

B-3. When returning the circuit board, place it inside a conductive plastic bag if available in order to protect the MOS devices from electrostatic discharge during shipment (The circuit board must NEVER be placed in contact with styrofoam materials). ENCLOSE a letter containing the following information with the returned circuit board.

Name, address, and phone number of purchaser
Date and place of purchase
Brief description of the difficulty

Mail a copy of this letter SEPARATELY to:

MOSTEK GMBH
Microcomputer Service Manager
Talstrasse 172
D 7024 Filderstadt - 1
West Germany

Securely package and mail the circuit board, prepaid and insured to:

MOSTEK GMBH
Microcomputer Service Department
Talstrasse 172
D 7024 Filderstadt - 1
West Germany

B-4. LIMITED WARRANTY.

B-5. MOSTEK warrants this product against defective materials and workmanship for a period of 90 days. This warranty does not apply to any product that has been subjected to misuse, accident, improper installation, improper application, or improper operation, nor does it apply to any product that has been repaired or altered by other than MOSTEK personnel. There are no warranties which extend beyond those herein specifically given.

MOSTEK®

EUROPEAN MARKETING OFFICES

MOSTEK INTERNATIONAL

150 CHAUSSEE DE LA HULPE
BRUSSELS B1170, BELGIUM
PHONES: (32) 02/660-2568/4713
TELEX: 62011 MKBRU B

SOUTHERN GERMANY

MOSTEK GMBH
TALSTRASSE 172
7024 FILDERSTADT-1 (BERNHAUSEN)
WEST GERMANY
PHONE: (49) 711 701045
TELEX: 7255792 MK D

NORTHERN GERMANY

MOSTEK GMBH
FRIEDLANDSTRASSEE 1
2085 QUICKBORN/HAMBURG
WEST GERMANY
PHONE: (49) 4106-2077/2078
TELEX: 213685 MKHA D

FRANCE

MOSTEK FRANCE S.A.R.L.
SILIC 217
F94518 RUGIS-CEDEX
FRANCE
PHONE: (33) 01/686-0153
TELEX: 204049 MOSTEKF

UNITED KINGDOM

MOSTEK UK, LTD.
1-3 VALLEY DRIVE
KINGSBURY ROAD
LONDON NW9, ENGLAND (UK)
PHONE: (44) 01-204-9322
TELEX: 25940 MOSTEK G

ITALY

MOSTEK ITALIA S.P.A.
VIA G. DA PROCIDA 10
I-20149 MILANO
ITALY
PHONE: (39) 02/3185337
TELEX: 25601 MOSTEK I

PRINTED IN USA March 1978
Publication No. MK78561